* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] In the parallel computer which consisted of two or more integrated circuits which can rewrite internal circuitry, and which can be reconfigurated and which can be reconfigurated The configuration setting table which described the number of implementation of the above-mentioned integrated circuit which performs predetermined processing and its processing, and which can be reconfigurated, A storage means by which the circuitry data for performing the above-mentioned predetermined processing described by this configuration setting table are memorized, The instruction control means which owns beforehand the data of the configuration of the above-mentioned integrated circuit which can be reconfigurated, and extracts the above-mentioned configuration setting table and the above-mentioned circuitry data from the above-mentioned storage means, From the above-mentioned instruction control means, the data, the above-mentioned configuration setting table, and the above-mentioned circuitry data of the configuration of the above-mentioned integrated circuit which can be reconfigurated Reception, It has the circuitry management tool which assigns the above-mentioned predetermined processing to the above-mentioned integrated circuit which can be reconfigurated. The parallel computer which is characterized by for the above-mentioned instruction control means writing the circuitry data for performing the above-mentioned predetermined processing in the above-mentioned integrated circuit which can be reconfigurated based on the quota result of the above-mentioned circuitry management tool, and making the above-mentioned integrated circuit which can be reconfigurated perform the above-mentioned predetermined processing and which can be reconfigurated.
[Claim 2] When a failure arises in either of the integrated circuits which can be reconfigurated, an instruction control means detects the above-mentioned failure. The data of the configuration of the integrated circuit with which the circuitry management tool included the above-mentioned failure from the above-mentioned instruction control means and which can be reconfigurated, The integrated circuit with which reception and the above-mentioned failure produced a configuration setting table and circuitry data and which can be reconfigurated is removed. Predetermined processing is newly assigned to the integrated circuit which can be reconfigurated. The above-mentioned instruction control means The parallel computer according to claim 1 which is characterized by writing the circuitry data for performing the above-mentioned predetermined processing in the above-mentioned integrated circuit which can be reconfigurated based on the new quota result of the above-mentioned circuitry management tool, and making the above-mentioned integrated circuit which can be reconfigurated perform the above-mentioned predetermined processing and which can be reconfigurated.
[Claim 3] The parallel computer according to claim 1 which is characterized by for a circuitry management tool giving a logical number to the integrated circuit which can be reconfigurated, and assigning predetermined processing to it based on the above-mentioned number and which can be reconfigurated.
[Claim 4] The 1st configuration setting table on which the number of implementation of the integrated circuit which can be reconfigurated which a storage means makes perform 1st predetermined processing and predetermined processing of the above 1st, and the 1st activation start time were described, The 2nd

configuration setting table on which the number of implementation of the above-mentioned integrated circuit which performs the 1st circuitry data for performing predetermined processing of the above 1st, 2nd predetermined processing, and predetermined processing of the above 2nd, and which can be reconfigurated, and the 2nd activation start time were described, The 2nd circuitry data for performing predetermined processing of the above 2nd is memorized. An instruction control means extracts the above 1st and the 2nd configuration setting table from the above-mentioned storage means. It is based at the 1st activation start time described by the configuration setting table of the above 1st. While the above-mentioned instruction control means extracts the circuitry data of the above 1st from the above-mentioned storage means and a circuitry management tool assigns predetermined processing of the above 1st to the above-mentioned integrated circuit which can be reconfigurated The operating condition of the above-mentioned integrated circuit which can be reconfigurated is held. The above-mentioned instruction control means The circuitry data of the above 1st are written in the assigned above-mentioned integrated circuit which can be reconfigurated. Make the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 1st, and it is based at the 2nd activation start time described at the configuration setting table of the above 2nd. The above-mentioned instruction control means extracts the circuitry data of the above 2nd from the above-mentioned storage means, and the above-mentioned circuitry management tool takes into consideration the operating condition of the above-mentioned integrated circuit which can be reconfigurated currently held. Predetermined processing of the above 2nd is assigned to the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means The parallel computer according to claim 1 which is characterized by writing the circuitry data of the above 2nd in the assigned above-mentioned integrated circuit which can be reconfigurated, and making the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 2nd and which can be reconfigurated.

[Claim 5] The 1st configuration setting table on which the number of implementation of the integrated circuit which can be reconfigurated which a storage means makes perform 1st predetermined processing and predetermined processing of the above 1st was described, The 2nd configuration setting table on which the number of implementation of the above-mentioned integrated circuit which performs 2nd predetermined processing and predetermined processing of the above 2nd, and which can be reconfigurated was described to be the 1st circuitry data for performing predetermined processing of the above 1st, The 2nd circuitry data for performing predetermined processing of the above 2nd is memorized. An instruction control means extracts the above 1st and the 2nd configuration setting table from the above-mentioned storage means. While the above-mentioned instruction control means extracts the circuitry data of the above 1st from the above-mentioned storage means and a circuitry management tool assigns predetermined processing of the above 1st to the above-mentioned integrated circuit which can be reconfigurated The operating condition of the above-mentioned integrated circuit which can be reconfigurated is held. The above-mentioned instruction control means The circuitry data of the above 1st are written in the assigned above-mentioned integrated circuit which can be reconfigurated. It is based on the processing information that make the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 1st, and predetermined processing of the above 1st is performed to it, from the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means extracts the circuitry data of the above 2nd from the above-mentioned storage means, and the above-mentioned circuitry management tool takes into consideration the operating condition of the above-mentioned integrated circuit which can be reconfigurated currently held. Predetermined processing of the above 2nd is assigned to the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means The parallel computer according to claim 1 which is characterized by writing the circuitry data of the above 2nd in the assigned above-mentioned integrated circuit which can be reconfigurated, and making the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 2nd and which can be reconfigurated.

[Claim 6] The 1st configuration setting table on which the number of implementation of the integrated

circuit which can be reconfigurated which a storage means makes perform 1st predetermined processing and predetermined processing of the above 1st was described, The 2nd configuration setting table on which the number of implementation of the above-mentioned integrated circuit which performs 2nd predetermined processing and predetermined processing of the above 2nd, and which can be reconfigurated was described to be the 1st circuitry data for performing predetermined processing of the above 1st, The 2nd circuitry data for performing predetermined processing of the above 2nd is memorized. An instruction control means extracts the above 1st and the 2nd configuration setting table from the above-mentioned storage means. The above-mentioned instruction control means extracts the circuitry data of the above 1st from the above-mentioned storage means. A circuitry management tool assigns predetermined processing of the above 1st to the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means writes the circuitry data of the above 1st in the assigned above-mentioned integrated circuit which can be reconfigurated. Make the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 1st, and the above-mentioned instruction control means extracts the circuitry data of the above 2nd from the above-mentioned storage means to it. The above-mentioned circuitry management tool takes into consideration the operating condition of the above-mentioned integrated circuit which can be reconfigurated notified from the above-mentioned instruction control means. Predetermined processing of the above 2nd is assigned to the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means The parallel computer according to claim 1 which is characterized by writing the circuitry data of the above 2nd in the assigned above-mentioned integrated circuit which can be reconfigurated, and making the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 2nd and which can be reconfigurated.

[Claim 7] On the configuration setting table which two or more integrated circuits which can be reconfigurated interconnect, and is memorized by the storage means The connection relation of two or more continuous predetermined processings is described, and the data of a configuration of that the instruction control means included the above-mentioned interconnect of the above-mentioned integrated circuit which can be reconfigurated are owned beforehand. The connection relation of two or more continuous predetermined processings in which the circuitry management tool is described by the above-mentioned configuration setting table, The parallel computer according to claim 1 which is characterized by assigning two or more predetermined processings which carried out [above-mentioned] continuation to the above-mentioned integrated circuit which can be reconfigurated in consideration of the above-mentioned interconnect of the above-mentioned integrated circuit which the above-mentioned instruction control means owns, and which can be reconfigurated and which can be reconfigurated.

[Claim 8] The configuration setting table on which a storage means is between the connection relation of two or more continuous predetermined processings and the processing which carried out [above-mentioned] continuation of predetermined [two or more], and the required bit width of face at the time of passing data is described is memorized. The data of a configuration of that the instruction control means contained the bit width of face of interconnect of the integrated circuit which can be reconfigurated are owned beforehand. The required bit width of face at the time of a circuitry management tool being between the processings in which two or more continuous predetermined processings described by the above-mentioned configuration setting table carried out connection relation and the above-mentioned continuation of predetermined [two or more], and passing data, The parallel computer according to claim 7 which is characterized by assigning two or more predetermined processings which carried out [above-mentioned] continuation to the above-mentioned integrated circuit which can be reconfigurated in consideration of the bit width of face of the above-mentioned interconnect of the above-mentioned integrated circuit which the above-mentioned instruction control means owns, and which can be reconfigurated and which can be reconfigurated.

[Claim 9] The configuration setting table on which the storage means described two or more numbers of implementation of the integrated circuit which performs predetermined processing and its processing, and which can be reconfigurated, Memorize the data of the logical circuit for performing the above-

mentioned predetermined processing, and the data of an I/O circuit, and a circuitry management tool corresponds to two or more above-mentioned numbers of implementation. The above-mentioned predetermined processing is assigned to two or more above-mentioned integrated circuits which can be reconfigurated. An instruction control means The parallel computer according to claim 8 which is characterized by writing the same logical circuit in them to the same processing in case the above-mentioned logical circuit and the above-mentioned I/O circuit are written in two or more integrated circuits to which the above-mentioned predetermined processing was assigned, and which can be reconfigurated and which can be reconfigurated.

[Claim 10] The parallel computer according to claim 9 which is characterized by assigning the above-mentioned integrated circuit with the wide bit width of face of interconnect which can be reconfigurated in case a circuitry management tool assigns predetermined processing to the integrated circuit which can be reconfigurated and which can be reconfigurated.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the parallel computer which consisted of two or more integrated circuits which can rewrite internal circuitry, and which can be reconfigurated and which can be reconfigurated.
[0002]
[Description of the Prior Art] The high-speed operation engine performance is needed in specific applications, such as digital signal processing, and an image processing, a complicated mathematical operation. In such a case, the general-purpose microprocessor of the operation engine performance is inadequate. Moreover, although sufficient operation engine performance will be obtained if the hardware of dedication, such as a custom-made processor, is used, flexible modification of an algorithm etc. is impossible and the design cycle has the fault that it is long and expensive.
[0003] Integrated circuits which can be reconfigurated, such as FPGA (Field Programmable GateArray) which uses SRAM (Static Random Access Memory) etc. as a storage element, consist of a combinational circuit which consists of AND, OR, etc. on 1 chip, a logical block which can realize a flip-flop etc., and a wiring block which makes connection between these logical blocks hold to storage elements, such as SRAM. Therefore, by giving the data of the storage element of a wiring block from the outside as circuitry data, connection between logical blocks can be made and an internal component circuit can be rewritten any number of times dynamically.
[0004] Therefore, it is possible for the operation engine performance higher than a general-purpose microprocessor to be obtained, and to change an algorithm flexibly, and how to obtain the operation engine performance of the purpose is considered, using integrated circuits which can be reconfigurated, such as FPGA, two or more. The thing as shown below is indicated about the parallel computer using such two or more FPGA.
[0005] drawing 13 -- the Patent Publication Heisei No. 502985 [four to] official report -- "-- the approach using the gate array logic which can be reconfigurated electrically -- and Are drawing showing the configuration of the conventional parallel computer which was indicated by the equipment constituted by this" (following, reference 1), and which can be reconfigurated, and it sets to drawing. 81 is the parallel computer which can be reconfigurated. Two or more logic chips 91-94, a memory module 95, the user setting module 96 and the above-mentioned logic chips 91-94, a memory module 95, and the user setting module 96 It is constituted by the interconnect chip 97 which makes arbitration interconnect. The host computer 82 is controlling the hardware configuration of the parallel computer 81 which can be reconfigurated, and its actuation through a host interface 83 and the configuration system 84.
[0006] The equipment which consists of an integrated circuit of the logic chip 91 of N individual connected mutually - 94 grades which can be reconfigurated as shown in drawing 13 is constituted from reference 1, the logical circuit data which should be carried in the integrated circuit which can be reconfigurated are divided into N individual, these data are assigned to the corresponding gate array

which can be reconfigurated, it writes in, and the method of making it operate is indicated.
[0007] Moreover, the equipment which consists of two or more integrated circuits which can be reconfigurated is constituted from "the processing unit, system, and approach" (following, reference 2) of JP,8-286908,A that it can reset freely dynamically, and while performing processing, the approach of writing in the integrated circuit which can be reconfigurated dynamically with the instruction from a program is indicated.
[0008]
[Problem(s) to be Solved by the Invention] Since the conventional parallel computer which can be reconfigurated is constituted as mentioned above, one processing and operation which are expressed in a digital logic network With the technique of the above-mentioned reference 1 supplied to two or more integrated circuits which can be reconfigurated When two or more different processings were performed to coincidence and these processings were supplied to two or more integrated circuits which can be reconfigurated, directions had to be given for every processing and the same or the technical problem that assignment could not be determined automatically occurred.
[0009] Moreover, circuitry data were divided into N individual and the technical problem that could divide data and they could not necessarily be assigned to N individual depending on circuitry data and the connection configuration between [which can be reconfigurated] integrated circuits occurred with the technique of the above-mentioned reference 1 which assigns those data to each integrated circuit which can be reconfigurated.
[0010] Furthermore, when adding and performing processing which is further different while performing two or more processings by assignment from a program with the technique of the above-mentioned reference 2 change dynamically the circuitry of the integrated circuit which can be reconfigurated, in order to assign processing to the integrated circuit which is not used and which can be reconfigurated, a certain assignment by the user was needed, and the technical problem that the integrated circuit which can be reconfigurated cannot be used efficiently was.
[0011] This invention was made in order to solve the above technical problems, and while performing automatically assignment to the integrated circuit of two or more different processings which can be reconfigurated, it carries out dynamically according to the connection configuration and the operating condition between [which can be reconfigurated] integrated circuits, and it aims at the same or obtaining the parallel computer which utilizes effectively each integrated circuit which can be reconfigurated and which can be reconfigurated in the equipment which consisted of two or more integrated circuits which can be reconfigurated.
[0012] Moreover, it aims at obtaining the parallel computer which enables use of equipment and which can be reconfigurated, without a user being conscious of assignment to the integrated circuit which can be reconfigurated.
[0013]
[Means for Solving the Problem] In what consisted of two or more integrated circuits with which the parallel computer concerning this invention which can be reconfigurated can rewrite internal circuitry, and which can be reconfigurated The configuration setting table which described the number of implementation of the above-mentioned integrated circuit which performs predetermined processing and its processing, and which can be reconfigurated, A storage means by which the circuitry data for performing the above-mentioned predetermined processing described by this configuration setting table are memorized, The instruction control means which owns beforehand the data of the configuration of the above-mentioned integrated circuit which can be reconfigurated, and extracts the above-mentioned configuration setting table and the above-mentioned circuitry data from the above-mentioned storage means, From the above-mentioned instruction control means, the data, the above-mentioned configuration setting table, and the above-mentioned circuitry data of the configuration of the above-mentioned integrated circuit which can be reconfigurated Reception, It has the circuitry management tool which assigns the above-mentioned predetermined processing to the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means writes the circuitry data for performing the above-mentioned predetermined processing in the above-mentioned integrated

circuit which can be reconfigurated based on the quota result of the above-mentioned circuitry management tool, and the above-mentioned integrated circuit which can be reconfigurated is made to perform the above-mentioned predetermined processing.

[0014] When a failure arises in either of the integrated circuits which can be reconfigurated, the parallel computer concerning this invention which can be reconfigurated An instruction control means detects the above-mentioned failure. A circuitry management tool from the above-mentioned instruction control means The data, the configuration setting table, and circuitry data of the configuration of the integrated circuit including the above-mentioned failure which can be reconfigurated Reception, Except for the integrated circuit which the above-mentioned failure produced and which can be reconfigurated, predetermined processing is newly assigned to the integrated circuit which can be reconfigurated. The above-mentioned instruction control means writes the circuitry data for performing the above-mentioned predetermined processing in the above-mentioned integrated circuit which can be reconfigurated based on the new quota result of the above-mentioned circuitry management tool, and the above-mentioned integrated circuit which can be reconfigurated is made to perform the above-mentioned predetermined processing.

[0015] The parallel computer concerning this invention which can be reconfigurated gives a number with a circuitry management tool logical to the integrated circuit which can be reconfigurated, and predetermined processing is assigned based on the above-mentioned number.

[0016] The 1st configuration setting table on which the number of implementation of the integrated circuit with which, as for the parallel computer concerning this invention which can be reconfigurated, a storage means performs 1st predetermined processing and predetermined processing of the above 1st, and which can be reconfigurated, and the 1st activation start time were described, The 2nd configuration setting table on which the number of implementation of the above-mentioned integrated circuit which performs the 1st circuitry data for performing predetermined processing of the above 1st, 2nd predetermined processing, and predetermined processing of the above 2nd, and which can be reconfigurated, and the 2nd activation start time were described, The 2nd circuitry data for performing predetermined processing of the above 2nd is memorized. An instruction control means extracts the above 1st and the 2nd configuration setting table from the above-mentioned storage means. It is based at the 1st activation start time described by the configuration setting table of the above 1st. While the above-mentioned instruction control means extracts the circuitry data of the above 1st from the above-mentioned storage means and a circuitry management tool assigns predetermined processing of the above 1st to the above-mentioned integrated circuit which can be reconfigurated The operating condition of the above-mentioned integrated circuit which can be reconfigurated is held. The above-mentioned instruction control means The circuitry data of the above 1st are written in the assigned above-mentioned integrated circuit which can be reconfigurated. Make the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 1st, and it is based at the 2nd activation start time described at the configuration setting table of the above 2nd. The above-mentioned instruction control means extracts the circuitry data of the above 2nd from the above-mentioned storage means, and the above-mentioned circuitry management tool takes into consideration the operating condition of the above-mentioned integrated circuit which can be reconfigurated currently held. Predetermined processing of the above 2nd is assigned to the above-mentioned integrated circuit which can be reconfigurated, and the above-mentioned instruction control means writes the circuitry data of the above 2nd in the assigned above-mentioned integrated circuit which can be reconfigurated, and makes the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 2nd.

[0017] The 1st configuration setting table on which the number of implementation of the integrated circuit with which, as for the parallel computer concerning this invention which can be reconfigurated, a storage means performs 1st predetermined processing and predetermined processing of the above 1st, and which can be reconfigurated was described, The 2nd configuration setting table on which the number of implementation of the above-mentioned integrated circuit which performs 2nd predetermined processing and predetermined processing of the above 2nd, and which can be reconfigurated was

described to be the 1st circuitry data for performing predetermined processing of the above 1st, The 2nd circuitry data for performing predetermined processing of the above 2nd is memorized. An instruction control means extracts the above 1st and the 2nd configuration setting table from the above-mentioned storage means. While the above-mentioned instruction control means extracts the circuitry data of the above 1st from the above-mentioned storage means and a circuitry management tool assigns predetermined processing of the above 1st to the above-mentioned integrated circuit which can be reconfigurated The operating condition of the above-mentioned integrated circuit which can be reconfigurated is held. The above-mentioned instruction control means The circuitry data of the above 1st are written in the assigned above-mentioned integrated circuit which can be reconfigurated. It is based on the processing information that make the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 1st, and predetermined processing of the above 1st is performed to it, from the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means extracts the circuitry data of the above 2nd from the above-mentioned storage means, and the above-mentioned circuitry management tool takes into consideration the operating condition of the above-mentioned integrated circuit which can be reconfigurated currently held. Predetermined processing of the above 2nd is assigned to the above-mentioned integrated circuit which can be reconfigurated, and the above-mentioned instruction control means writes the circuitry data of the above 2nd in the assigned above-mentioned integrated circuit which can be reconfigurated, and makes the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 2nd.

[0018] The 1st configuration setting table on which the number of implementation of the integrated circuit with which, as for the parallel computer concerning this invention which can be reconfigurated, a storage means performs 1st predetermined processing and predetermined processing of the above 1st, and which can be reconfigurated was described, The 2nd configuration setting table on which the number of implementation of the above-mentioned integrated circuit which performs 2nd predetermined processing and predetermined processing of the above 2nd, and which can be reconfigurated was described to be the 1st circuitry data for performing predetermined processing of the above 1st, The 2nd circuitry data for performing predetermined processing of the above 2nd is memorized. An instruction control means extracts the above 1st and the 2nd configuration setting table from the above-mentioned storage means. The above-mentioned instruction control means extracts the circuitry data of the above 1st from the above-mentioned storage means. A circuitry management tool assigns predetermined processing of the above 1st to the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means writes the circuitry data of the above 1st in the assigned above-mentioned integrated circuit which can be reconfigurated. Make the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 1st, and the above-mentioned instruction control means extracts the circuitry data of the above 2nd from the above-mentioned storage means to it. The above-mentioned circuitry management tool takes into consideration the operating condition of the above-mentioned integrated circuit which can be reconfigurated notified from the above-mentioned instruction control means. Predetermined processing of the above 2nd is assigned to the above-mentioned integrated circuit which can be reconfigurated, and the above-mentioned instruction control means writes the circuitry data of the above 2nd in the assigned above-mentioned integrated circuit which can be reconfigurated, and makes the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 2nd.

[0019] As for the parallel computer concerning this invention which can be reconfigurated, two or more integrated circuits which can be reconfigurated interconnect. The connection relation of two or more predetermined processings which followed the configuration setting table memorized by the storage means is described. The connection relation of two or more continuous predetermined processings in which own beforehand the data of a configuration of that the instruction control means included the above-mentioned interconnect of the above-mentioned integrated circuit which can be reconfigurated, and the circuitry management tool is described by the above-mentioned configuration setting table, In consideration of the above-mentioned interconnect of the above-mentioned integrated circuit which the

above-mentioned instruction control means owns and which can be reconfigurated, two or more predetermined processings which carried out [above-mentioned] continuation are assigned to the above-mentioned integrated circuit which can be reconfigurated.
[0020] The connection relation of two or more predetermined processings in which, as for the parallel computer concerning this invention which can be reconfigurated, the storage means continued, The configuration setting table on which it is between the processings which carried out [above-mentioned] continuation of predetermined [two or more], and the required bit width of face at the time of passing data is described is memorized. The data of a configuration of that the instruction control means contained the bit width of face of interconnect of the integrated circuit which can be reconfigurated are owned beforehand. The required bit width of face at the time of a circuitry management tool being between the processings in which two or more continuous predetermined processings described by the above-mentioned configuration setting table carried out connection relation and the above-mentioned continuation of predetermined [two or more], and passing data, In consideration of the bit width of face of the above-mentioned interconnect of the above-mentioned integrated circuit which the above-mentioned instruction control means owns and which can be reconfigurated, two or more predetermined processings which carried out [above-mentioned] continuation are assigned to the above-mentioned integrated circuit which can be reconfigurated.
[0021] The configuration setting table on which, as for the parallel computer concerning this invention which can be reconfigurated, the storage means described two or more numbers of implementation of the integrated circuit which performs predetermined processing and its processing, and which can be reconfigurated, Memorize the data of the logical circuit for performing the above-mentioned predetermined processing, and the data of an I/O circuit, and a circuitry management tool corresponds to two or more above-mentioned numbers of implementation. The above-mentioned predetermined processing is assigned to two or more above-mentioned integrated circuits which can be reconfigurated, and in case an instruction control means writes the above-mentioned logical circuit and the above-mentioned I/O circuit in two or more integrated circuits to which the above-mentioned predetermined processing was assigned and which can be reconfigurated, the same logical circuit is written in to the same processing.
[0022] The parallel computer concerning this invention which can be reconfigurated is assigned to the above-mentioned integrated circuit with the wide bit width of face of interconnect which can be reconfigurated in case a circuitry management tool assigns predetermined processing to the integrated circuit which can be reconfigurated.
[0023]
[Embodiment of the Invention] Hereafter, one gestalt of implementation of this invention is explained. Gestalt 1. drawing 1 of operation is drawing showing the configuration of the parallel computer by the gestalt 1 of implementation of this invention which can be reconfigurated. In drawing 1 , 1 is an instruction control means which the parallel computer which can be reconfigurated, and 11-18 give the integrated circuit (FPGA) of plurality (eight [in this case,]) which can be reconfigurated to the integrated circuits 11-18 which can be reconfigurated, and 2 gives control instruction and data, and controls actuation, and 100 is a bus signal line which performs communication link actuation which includes data transfer and circuit information transfer between the integrated circuits 11-18 which can be reconfigurated, and the instruction control means 2.
[0024] Moreover, in drawing 1 , 4 is a storage means by which the configuration setting table which described the number of the integrated circuits which perform predetermined processing and its processing, and which can be reconfigurated (the number of implementation), and the circuitry data for performing predetermined processing described by this configuration setting table are memorized. Drawing 2 is drawing showing the configuration setting table 51, and the number of the integrated circuits which perform predetermined processing and its processing and which can be reconfigurated (the number of implementation) is described. Moreover, the circuitry data memorized by the storage means 4 are wiring connection data between the logical blocks inside a certain integrated circuit which can be reconfigurated, and the predetermined circuit which performs predetermined processing to those

integrated circuits 11-18 that can be reconfigurated is realized by writing this circuitry data in the integrated circuits 11-18 which can be reconfigurated.
[0025] Furthermore, in drawing 1 , 3 is a circuitry management tool which determines the suitable assignment to the integrated circuits 11-18 of reception and predetermined processing of the configuration setting table and circuitry data which are memorized by the storage means 4, and the data of the configuration of the integrated circuit 11-18 which the instruction control means 2 owns beforehand, and which can be reconfigurated which can be reconfigurated. 111 is a signal line which delivers the information memorized by the storage means 4 to the instruction control means 2.
[0026] Next, actuation is explained. First, the instruction control means 2 extracts the configuration setting table 51 shown in drawing 2 from the storage means 4 at the time of starting of this parallel computer 1 that can be reconfigurated. Next, the instruction control means 2 extracts the circuitry data for performing each predetermined processing described by the configuration setting table 51 from the storage means 4.
[0027] Then, the circuitry management tool 3 determines reception and everywhere assignment to the integrated circuits 11-18 of processing of a law which can be reconfigurated from the instruction control means 2 for the configuration setting table 51 extracted from the storage means 4, circuitry data, and the data of the configuration of the integrated circuit 11-18 which the instruction control means 2 owns beforehand and which can be reconfigurated. The instruction control means 2 writes the circuitry data for [which the circuitry management tool 3 determined] assigning and performing each predetermined processing based on a result in each integrated circuits 11-18 which can be reconfigurated.
[0028] After the writing of the circuitry data to each integrated circuits 11-18 which can be reconfigurated is performed, the instruction control means 2 supplies suitable data and a clock of operation, and makes each integrated circuits 11-18 which can be reconfigurated perform predetermined processing to the integrated circuits 11-18 to which predetermined processing was assigned and which can be reconfigurated based on the quota result of the circuitry management tool 3.
[0029] Thus, when the circuitry management tool 3 assigns predetermined processing to the suitable integrated circuits 11-18 which can be reconfigurated in consideration of the configuration of the integrated circuits 11-18 which can be reconfigurated and the instruction control means 2 writes in the integrated circuits 11-18 which can be reconfigurated for the circuitry data for performing predetermined processing, the parallel computer which performs predetermined processing and which can be reconfigurated is realized automatically.
[0030] Although the above-mentioned example is an example at the time of starting of the parallel computer 1 which can be reconfigurated Moreover, the circuit to realize is changed after starting the parallel computer 1 which can be reconfigurated. By preparing another configuration setting table and circuitry data, and performing the same procedure as the time of starting of the parallel computer 1 which can be reconfigurated, when making another predetermined processing perform The circuitry data for performing assignment of another predetermined processing and another predetermined processing are again written in to each integrated circuits 11-18 which can be reconfigurated. Thereby, after starting can write in the circuitry data to each integrated circuits 11-18 which can be reconfigurated.
[0031] Moreover, after the time of starting, or starting, when a failure arises in either of the integrated circuits 11-18 which can be reconfigurated, the instruction control means 2 detects this failure, and should just perform assignment of predetermined processing, and the writing of circuitry data in the above-mentioned procedure again. The writing to the integrated circuits 11-18 of circuitry data which can be reconfigurated can be performed without being influenced by this, according to the failure of the integrated circuits 11-18 which can be reconfigurated etc., even if it is the case where modification arises in a configuration.
[0032] For example, in the case of the configuration setting table 51 shown in drawing 2 , it is the example which realizes predetermined processing 61 with five integrated circuits which can be reconfigurated, and realizes predetermined processing 62 with two integrated circuits which can be reconfigurated, and as long as this condition is fulfilled, the circuitry management tool 3 determines assignment freely. As an example of the technique of assignment, the circuitry management tool 3 gives

a logical number to the integrated circuits 11-18 which can be reconfigurated, and can consider how to assign predetermined processing to order with a small number. By this technique, when realizing with the configuration of the parallel computer 1 which shows the configuration setting table 51 shown in drawing 2 to drawing 1 and which can be reconfigurated, the predetermined processing 61 is assigned to the integrated circuits 11-15 which can be reconfigurated, the predetermined processing 62 is assigned to the integrated circuits 16 and 17 which can be reconfigurated, and the circuitry data which correspond, respectively are written in.

[0033] Moreover, for example, when a failure occurs in the integrated circuit 14 which can be reconfigurated, the circuitry management tool 3 assigns the predetermined processing 61 to the integrated circuits 11-13 which can be reconfigurated, and 15 and 16 except for the integrated circuit 14 which can be reconfigurated, the predetermined processing 62 is assigned to the integrated circuits 17 and 18 which can be reconfigurated, and the instruction control means 2 writes in the circuitry data which correspond, respectively.

[0034] As mentioned above, the effectiveness that the parallel computer which can be reconfigurated can be used is acquired, without a user being conscious of assignment to the integrated circuit which can be reconfigurated by the circuitry management tool's 3 assigning two or more same or different predetermined processings automatically to the integrated circuit which can be reconfigurated, and writing in the circuitry data for performing predetermined processing to each integrated circuits 11-18 which can be reconfigurated, respectively according to the gestalt 1 of this operation.

[0035] Moreover, the effectiveness that each integrated circuits 11-18 which can be reconfigurated are effectively utilizable is acquired by changing the circuit to realize, and performing the same assignment and the same writing, when making another predetermined processing perform, or also when a failure occurs in the integrated circuits 11-18 which can be reconfigurated after starting the parallel computer 1 which can be reconfigurated.

[0036] gestalt 2. of operation -- at the time of use of the parallel computer 1 which can be reconfigurated, the gestalt 2 of implementation of this invention adds circuitry data, and is realized. Drawing 3 and drawing 4 are drawings showing the configuration setting tables 52 and 53 which described the number of implementation which realizes predetermined processings and those processings, and the activation start time which starts activation of a configuration setting table is described by each configuration setting tables 52 and 53. From this activation start time, it shall assign and writing and predetermined processing shall be performed.

[0037] The configuration of the parallel computer 1 in the gestalt 2 of this operation which can be reconfigurated is the same as the configuration shown in drawing 1 of the gestalt 1 of operation, and the circuitry data for carrying out predetermined processings 63-65 described by the configuration setting tables 52 and 53 and the configuration setting table to the storage means 4 are memorized.

[0038] Next, actuation is explained. First, the instruction control means 2 extracts the configuration setting tables 52 and 53 from the storage means 4 at the time of starting of this parallel computer 1 that can be reconfigurated. Since the activation start time described by the configuration setting table 52 is 0, it sets to time amount 0. Next, the instruction control means 2 The circuitry data for performing predetermined processings 63 and 64 described by the configuration setting table 52 shown in drawing 3 are extracted from the storage means 4, by the same procedure as the gestalt 1 of operation, assignment of predetermined processing and the writing of circuitry data are performed, and processing of a law is performed everywhere. And in case the instruction control means 2 writes in, the circuitry management tool 3 holds the operating condition of each integrated circuits 11-18 which can be reconfigurated.

[0039] Next, since the activation start time described by the configuration setting table 53 is 100, in time amount 100, the instruction control means 2 extracts the circuitry data for performing predetermined processing 65 described by the configuration setting table 53 shown in drawing 4 from the storage means 4. Then, the circuitry management tool 3 assigns the predetermined processing 65 to the integrated circuits 11-18 which are not using the circuitry data for performing the configuration setting table 53 and predetermined processing 65 from the instruction control means 2 in consideration of the operating condition of reception and each integrated circuits 11-18 which are held, and which can be

reconfigurated and which can be reconfigurated. The instruction control means 2 writes in the circuitry data only corresponding to the integrated circuits 11-18 with which assignment was performed and which can be reconfigurated based on the quota result of the circuitry management tool 3. After writing is performed, each predetermined processing is performed.

[0040] Moreover, activation initiation of each configuration setting tables 52 and 53 may specify it that activation initiation of each configuration setting table is performed by some conditions rather than may specify time amount. For example, in the above-mentioned example, the configuration of the configuration setting table 52 is realized and suppose that predetermined processings 63 and 64 were performed. In this case, when the predetermined processing 63 is completed, the instruction control means 2 may be made to realize the contents which extract that information from the storage means 4, and are described [information] by the configuration setting table 53 in reception and the configuration setting table 53. Moreover, for example, the signal of the processing termination from one of the integrated circuits 11-18 which can be reconfigurated may be specified that activation initiation of a configuration setting table is performed a condition [what the instruction control means 2 receives].

[0041] Moreover, you may make it start activation of each configuration setting tables 52 and 53 according to specific time amount, or not conditions but the operating condition of the integrated circuits 11-18 which can be reconfigurated. The configuration setting table 52 shown in the configuration setting table 54 shown in drawing 5 instead of and drawing 3 is memorized to the storage means 4, and drawing 5 performs the configuration setting table 54 after the configuration setting table 52. [the configuration setting table 53 which is drawing showing the configuration setting table 54, and is shown in above-mentioned drawing 4]

[0042] In this case, the processing 63 predetermined by time amount 0 is assigned to three pieces, the predetermined processing 64 is assigned to two pieces and the integrated circuits 11-18 which can be reconfigurated, and it performs. Next, since the activation start time described by the configuration setting table 54 is 1, by time amount 1, the configuration setting table 54 is performed and the predetermined processing 66 is assigned to five pieces and the integrated circuits 11-18 which can be reconfigurated. However, since there are only three intact integrated circuits 11-18 which can be reconfigurated when the processing 63 predetermined in this time or 64 is not completed, the predetermined processing 66 cannot be assigned.

[0043] In this case, activation of the configuration setting table 54 is interrupted by the circuitry management tool 3. Then, termination of predetermined processing 63 or the predetermined, predetermined processing 64 sends the information about the operating condition of the integrated circuits 11-18 which can be reconfigurated from the instruction control means 2 to the circuitry management tool 3. Since the number of the intact integrated circuits 11-18 which can be reconfigurated becomes five or more about the operating condition of the integrated circuits 11-18 which are held with the circuitry management tool 3 and which can be reconfigurated at this time, by the circuitry management tool 3, activation of the configuration setting table 54 is resumed and assignment is performed.

[0044] The writing to the integrated circuits 11-18 of the circuitry data corresponding to the operating condition of the integrated circuits 11-18 which can be reconfigurated etc. which can be reconfigurated can be performed by this, the integrated circuits 11-18 which can be reconfigurated can be used effectively, and a user can use the parallel computer which can be reconfigurated, without being conscious of the integrated circuits 11-18 to assign and which can be reconfigurated.

[0045] While using the parallel computer which can be reconfigurated, according to the gestalt 2 of this operation, the circuitry management tool 3 as mentioned above, according to predetermined time amount and predetermined conditions Moreover, when predetermined processing is assigned to the suitable integrated circuits 11-18 which can be reconfigurated and the instruction control means 2 writes in circuitry data according to the operating condition of the integrated circuits 11-18 which can be reconfigurated While being able to assign predetermined processing automatically to the integrated circuits 11-18 which can be reconfigurated and being able to utilize effectively each integrated circuits 11-18 which can be reconfigurated, a user The effectiveness which can use the parallel computer which

can be reconfigurated and to say is acquired without being conscious of the integrated circuits 11-18 to assign and which can be reconfigurated.
[0046] Gestalt 3. drawing 6 of operation is drawing showing the configuration of the parallel computer by the gestalt 3 of implementation of this invention which can be reconfigurated. As shown in drawing, between [of specification / which can be reconfigurated] integrated circuits 11-18 is connected, and one arithmetic circuit consists of combining two or more circuitry data. In drawing 6 , the parallel computer 1 which can be reconfigurated has two or more of the same integrated circuits 11-18 as drawing 1 of the gestalt 1 of operation which can be reconfigurated, the instruction control means 2, the circuitry management tool 3, the storage means 4, and a signal line 100,111. Moreover, in drawing 6 , communication link actuation including data transfer is performed through signal lines 101-110 the integrated circuit 11 which can be reconfigurated - between 18.
[0047] Drawing 7 is drawing showing the configuration setting table 55 which described the number of implementation which realizes a series of predetermined processings and those processings, and the circuitry data for carrying out predetermined processings 67, 68, 69, 70, and 71 described by this configuration setting table 55 and the configuration setting table 55 to the storage means 4 are memorized.
[0048] Next, actuation is explained. First, the instruction control means 2 extracts the configuration setting table 55 shown in drawing 7 from the storage means 4 at the time of starting of this parallel computer 1 that can be reconfigurated. Next, the instruction control means 2 extracts the circuitry data for performing each predetermined processing described by the configuration setting table 55 from the storage means 4. Then, the circuitry management tool 3 determines everywhere assignment to the integrated circuits 11-18 of processing of a law which can be reconfigurated from the instruction control means 2 based on reception and those information for the configuration setting table 55, circuitry data, the data of the configuration of the integrated circuit 11-18 which the instruction control means 2 owns beforehand and which can be reconfigurated, and the information on connection of each mutual. Subsequent processing is the same as the case of the gestalt 1 of operation.
[0049] For example, after inputting and performing the data from the instruction control means 2 to the predetermined processing 67 in the case of drawing 7 , The output is passed and performed to the predetermined processing 68 and the predetermined processing 69. The output of the predetermined processings 68 and 69 It is the example which passes and performs to the predetermined processing 70, realizes continuous processing in which an output is passed to the instruction control means 2, with the one-set integrated circuit which can be reconfigurated, and realizes predetermined processing 71 with three integrated circuits which can be reconfigurated.
[0050] The circuitry management tool 3 divides and hits the integrated circuits 11-18 which can be reconfigurated in each circuitry data for performing predetermined processings 67-71 under the connection-related constraint of the predetermined processings 67-70, the constraint which assigns one set of configurations which the predetermined processings 67-70 followed, and the constraint of assigning three predetermined processings 71. As an example, the predetermined processing 67 to the integrated circuit 11 which can be reconfigurated the predetermined processing 68 to the integrated circuit 12 which can be reconfigurated The integrated circuit 13 which can be reconfigurated, and the predetermined processing 71 to 14 and 17 the predetermined processing 69 to the integrated circuit 15 which can be reconfigurated Assignment which fulfilled the above-mentioned constraint can be performed by distributing predetermined processing so that it may say that the predetermined processing 70 is assigned to the integrated circuit 16 which can be reconfigurated, and predetermined processing is not assigned to the integrated circuit 18 which can be reconfigurated.
[0051] the activity which assigns circuitry data to the integrated circuits 11-18 which can be reconfigurated based on such conditions -- mathematical -- "-- conditional -- it is formulized as maximum minimum problem." About the solution method of such a problem, much technique is proposed from the former and which technique may be used at the quota process of this invention. Thereby, by combining two or more circuitry data, when one arithmetic circuit is realized, in consideration of connection between [which can be reconfigurated] integrated circuits 11-18, circuitry

data can be written in the suitable integrated circuits 11-18 which can be reconfigurated.
[0052] According to the gestalt 3 of this operation, by as mentioned above, the thing for which two or more circuitry data are combined When one arithmetic circuit is realized, the circuitry management tool 3 determines assignment of predetermined processing in consideration of connection between [which can be reconfigurated] integrated circuits 11-18. When the instruction control means 2 writes circuitry data in the suitable integrated circuits 11-18 which can be reconfigurated, the effectiveness that each integrated circuits 11-18 which can be reconfigurated are effectively utilizable is acquired.
[0053] It is drawing showing the configuration of the parallel computer which can be reconfigurated according [gestalt 4. drawing 8 of operation] to the gestalt 4 of implementation of this invention, and as shown in drawing, between [of specification / which can be reconfigurated] integrated circuits 11-18 is connected, and the connection configuration to the exterior of the signal line in the integrated circuits 11-18 which can be reconfigurated changes with each integrated circuits 11-18 which can be reconfigurated. In drawing 8 , the parallel computer 1 which can be reconfigurated has two or more integrated circuits 11-18 which can be reconfigurated, instruction control means 2, circuitry management tools 3, and storage means 4 like drawing 6 of the gestalt 3 of operation. The integrated circuits 11-18 which can be reconfigurated perform communication link actuation including data transfer and circuit information transfer through the instruction control means 2 and a signal line 200. Moreover, the integrated circuit 11 which can be reconfigurated - between 18, communication link actuation including data transfer and circuit information transfer is performed through signal lines 201-210.
[0054] Moreover, signal lines 201-203,205,206,209 shall be eight pins for data I/O, and the signal line 204,207,208,210 shall consist of 16 pins for data I/O. For this reason, signal lines 201-203,205,206,209 are signal lines of 8-bit width of face, and a signal line 204,207,208,210 is considered to be the signal line of 16-bit width of face.
[0055] In case drawing 9 passes data by processing of a law the number of implementation, and everywhere which realizes a series of predetermined processings and those processings, it is drawing showing the configuration setting table 56 which described required bit width of face. The circuitry data for carrying out predetermined processings 72-75 described by the configuration setting table 56 and the configuration setting table 56 to the storage means 4 are memorized.
[0056] Next, actuation is explained. First, the instruction control means 2 extracts the configuration setting table 56 from the storage means 4 at the time of starting of this parallel computer 1 that can be reconfigurated. Next, the instruction control means 2 extracts the circuitry data for performing each predetermined processing described on the configuration setting table 56 from the storage means 4. Then, the circuitry management tool 3 determines everywhere assignment to the integrated circuits 11-18 of processing of a law which can be reconfigurated from the instruction control means 2 based on reception and those received information for the information on the data width of face of the configuration setting table 56, circuitry data, and the connection relation between [which can be reconfigurated] integrated circuits 11-18 and each signal line that the instruction control means 2 owns beforehand. Subsequent processing is the same as the case of the gestalt 1 of operation.
[0057] Thereby, when the connection configuration to the exterior of the signal line in the integrated circuits 11-18 which can be reconfigurated changes with each integrated circuits 11-18 which can be reconfigurated, in consideration of the data width of face of a signal line, circuitry data can be written in the suitable integrated circuit which can be reconfigurated.
[0058] For example, in the case of drawing 9 , it is the example which realizes continuous processing in which sequential execution activation of the predetermined processings 72-75 is carried out, with two pieces and the integrated circuit which can be reconfigurated. Moreover, in order to pass data to the predetermined processings 72-73 and the predetermined processings 73-74, the signal line of 16-bit width of face is required, and in order to pass data to the predetermined processings 74-75, the signal line of 8-bit width of face is needed. Moreover, from the instruction control means 2, the predetermined processing 72 must output reception to the instruction control means 2, and the predetermined processing 75 must output the data of a processing result for data.

[0059] Assignment which fulfilled the above-mentioned constraint can be performed by distributing predetermined processing as the predetermined processing 73 is assigned as an example to the integrated circuits 11 and 14 which can be reconfigurated for the predetermined processing 72 at the integrated circuits 15 and 18 which can be reconfigurated and the predetermined processing 75 is assigned to the integrated circuits 16 and 17 which can be reconfigurated for the predetermined processing 74 at the integrated circuits 12 and 13 which can be reconfigurated. Even if it is the case where the constraint about I/O with such data width of face and the exterior is added, the technique of assigning predetermined processing to the integrated circuits 11-18 which can be reconfigurated is the same as the gestalt 3 of operation, and good.
[0060] As mentioned above, even if it is the case where the constraint about I/O with the data width of face between [which can be reconfigurated] integrated circuits 11-18, and the exterior is added according to the gestalt 4 of this operation The circuitry management tool 3 by determining assignment of predetermined processing and writing circuitry data in the suitable integrated circuits [the instruction control means 2] 11-18 which can be reconfigurated in consideration of connection between [which can be reconfigurated] integrated circuits 11-18, and data width of face The effectiveness that each integrated circuits 11-18 which can be reconfigurated are effectively utilizable is acquired.
[0061] gestalt 5. of operation -- the configuration of the parallel computer 1 in the gestalt of this operation which can be reconfigurated is the same as drawing 8 of the gestalt 4 of operation. Drawing 10 is drawing showing the configuration setting table 57 which described two or more numbers of implementation which realize predetermined processings and those processings. The logical circuit data for performing predetermined processings 76 and 77 described by the configuration setting table 57 and the configuration setting table 57 and the I/O circuit data according to bit width of face are memorized by the storage means 4.
[0062] Drawing 11 is the mimetic diagram showing the relation of the logical circuit data for performing predetermined processings 76 and 77, and the I/O circuit data according to bit width of face. Since the number of implementation of the configuration setting table 57 shown in drawing 10 is 2, in drawing 11 , the logical circuits 21 and 24 for performing predetermined processing 76 are realized by the integrated circuits 11 and 14 which can be reconfigurated, and the logical circuits 25 and 28 for performing predetermined processing 77 are realized at the integrated circuits 15 and 18 which can be reconfigurated. Moreover, the I/O circuits 31, 35, 34, and 38 for 16-bit width of face (I/O circuit) are realized by the integrated circuits 11, 15, 14, and 18 which can be reconfigurated.
[0063] That is, when assigning the predetermined processing 76 to the integrated circuit 11 which can be reconfigurated and assigning the predetermined processing 77 to the integrated circuit 15 which can be reconfigurated, the instruction control means 2 compounds the logical circuit 21 for performing predetermined processing 76, and the I/O circuit 31 for 16 bit width of face, writes in the integrated circuit 11 which can be reconfigurated, compounds the logical circuit 25 for performing predetermined processing 77, and the I/O circuit 35 for 16 bit width of face, and writes in to the integrated circuit 15 which can be reconfigurated.
[0064] When similarly assigning the predetermined processing 76 to the integrated circuit 14 which can be reconfigurated and assigning the predetermined processing 77 to the integrated circuit 18 which can be reconfigurated, the instruction control means 2 compounds a logical circuit 24 and the I/O circuit 34 for 16-bit width of face, is written in the integrated circuit 14 which can be reconfigurated, compounds a logical circuit 28 and the I/O circuit 38 for 16-bit width of face, and writes them in the integrated circuit 18 which can be reconfigurated.
[0065] While exchanging the data of 16-bit width of face twice among the integrated circuits 11 and 15 which can be reconfigurated since the signal line of 32-bit width of face is needed for exchange of the data of the predetermined processings 76 and 77 as shown in the configuration setting table 57 of drawing 10 , the data of 16-bit width of face are exchanged twice among the integrated circuits 14 and 18 which can be reconfigurated. In this case, the logical circuits 21 and 24 corresponding to the predetermined processing 76 exchange data for the logical circuits 25 and 28 corresponding to the predetermined processing 77 through the I/O circuits 31 and 35 for 16-bit width of face, and the I/O

circuits 34 and 38 for 16-bit width of face, respectively.
[0066] Since the logical circuits 21 and 24 corresponding to the processing 76 predetermined to the above-mentioned case are common logical circuits and are logical circuits where the logical circuits 25 and 28 corresponding to the predetermined processing 77 are also common, By dividing and writing logical circuits 21, 25, 24, and 28 and the I/O circuits 31, 35, 34, and 38 for 16-bit width of face in the integrated circuits 11, 15, 14, and 18 which can be reconfigurated It is not necessary to create logical circuits 21 and 24 separately and to also create logical circuits 25 and 28 separately.
[0067] Drawing 12 is another mimetic diagram showing the relation of the logical circuit data for performing predetermined processings 76 and 77, and the I/O circuit data according to bit width of face. In drawing 12 , the logical circuits 22 and 23 corresponding to the predetermined processing 76 are realized by the integrated circuits 12 and 13 which can be reconfigurated, and the logical circuits 26 and 27 for performing predetermined processing 77 are realized at the integrated circuits 16 and 17 which can be reconfigurated. Moreover, the I/O circuits 32, 36, 33, and 37 for 8-bit width of face (I/O circuit) are realized by the integrated circuits 12, 16, 13, and 17 which can be reconfigurated.
[0068] Since the signal line of 32-bit width of face is needed for exchange of the data of the predetermined processings 76 and 77, the data of 8-bit width of face are exchanged by a unit of 4 times, respectively between the integrated circuits 12 and 16 which can be reconfigurated, and the integrated circuits 13 and 17 which can be reconfigurated. In this case, the logical circuits 22 and 23 for performing predetermined processing 76 exchange data for the logical circuits 26 and 27 for performing predetermined processing 77 through the I/O circuits 32, 36, 33, and 37 for 8-bit width of face, respectively.
[0069] Since the logical circuits 22 and 23 for performing predetermined processing 76 in the above-mentioned case are common logical circuits and are logical circuits where the logical circuits 26 and 27 for performing predetermined processing 77 are also common, By dividing and writing logical circuits 22, 26, 23, and 27 and the I/O circuits 32, 36, 33, and 37 for 8-bit width of face in the integrated circuits 12, 16, 13, and 17 which can be reconfigurated It is not necessary to create logical circuits 22 and 23 separately and to also create logical circuits 26 and 27 separately.
[0070] Moreover, when exchanging data by the predetermined processings 76 and 77, since the 16-bit width-of-face signal line can exchange many data at a time rather than a 8-bit width-of-face signal line, it is advantageous. The circuitry management tool 3 may assign circuitry data to the more advantageous integrated circuits 11-18 which can be reconfigurated based on the information on the bit width of face of such a signal line. In the above-mentioned example, the direction assigned, for example as shown in drawing 11 rather than drawing 12 can accelerate predetermined processing. Thus, predetermined processing is accelerable by assigning predetermined processing to the larger thing of the data-exchange capacity between [which can be reconfigurated] integrated circuits 11-18.
[0071] As mentioned above, according to the gestalt 5 of this operation, the effectiveness that it is not necessary to create a common logical circuit separately is acquired by dividing and writing a logical circuit and an I/O circuit in the integrated circuits 11-18 which can be reconfigurated.
[0072] Moreover, according to the gestalt 5 of this operation, when the circuitry management tool 3 assigns circuitry data to the large integrated circuits 11-18 of bit width of face which can be reconfigurated based on the information on the bit width of face of the signal line of the integrated circuits 11-18 which can be reconfigurated, the effectiveness that predetermined processing is accelerable is acquired.
[0073]
[Effect of the Invention] As mentioned above, the configuration setting table which described the number of implementation of the integrated circuit which can be reconfigurated which performs predetermined processing and its processing according to this invention, A storage means by which the circuitry data for performing predetermined processing described by this configuration setting table are memorized, The instruction control means which owns beforehand the data of the configuration of the integrated circuit which can be reconfigurated, and extracts a configuration setting table and circuitry data from a storage means, From an instruction control means, the data, the configuration setting table,

and circuitry data of the configuration of the integrated circuit which can be reconfigurated Reception, It has the circuitry management tool which assigns predetermined processing to the integrated circuit which can be reconfigurated. By an instruction control means's writing the circuitry data for performing predetermined processing in the integrated circuit which can be reconfigurated based on the quota result of a circuitry management tool, and making the integrated circuit which can be reconfigurated perform the above-mentioned predetermined processing It is effective in the ability to use the parallel computer which can be reconfigurated, without performing automatically assignment to the integrated circuit of predetermined processing which can be reconfigurated, and a user being conscious of assignment to the integrated circuit which can be reconfigurated.

[0074] When a failure arises in either of the integrated circuits which can be reconfigurated according to this invention An instruction control means detects a failure. A circuitry management tool from an instruction control means The data, the configuration setting table, and circuitry data of the configuration of the integrated circuit including a failure which can be reconfigurated Reception, Except for the integrated circuit which the failure produced and which can be reconfigurated, predetermined processing is newly assigned to the integrated circuit which can be reconfigurated. By an instruction control means's writing the circuitry data for performing predetermined processing in the integrated circuit which can be reconfigurated based on the new quota result of a circuitry management tool, and making the integrated circuit which can be reconfigurated perform the above-mentioned predetermined processing Also when a failure occurs in the integrated circuit which can be reconfigurated, it is effective in each integrated circuit which can be reconfigurated being effectively utilizable.

[0075] According to this invention, when a circuitry management tool gives a logical number to the integrated circuit which can be reconfigurated and assigns predetermined processing to it based on a number, it is effective in the ability to assign predetermined processing easily to the integrated circuit which can be reconfigurated.

[0076] According to this invention, an instruction control means extracts the 1st and 2nd configuration setting tables from a storage means. While an instruction control means extracts the 1st circuitry data from a storage means and a circuitry management tool assigns the 1st predetermined processing to the integrated circuit which can be reconfigurated based on the 1st activation start time described by the 1st configuration setting table Hold the operating condition of the integrated circuit which can be reconfigurated and an instruction control means writes the 1st circuitry data in the assigned above-mentioned integrated circuit which can be reconfigurated. Make the integrated circuit which can be reconfigurated perform 1st predetermined processing, and it is based at the 2nd activation start time described at the 2nd configuration setting table. An instruction control means extracts the 2nd circuitry data from a storage means, and a circuitry management tool takes into consideration the operating condition of the integrated circuit which can be reconfigurated currently held. When the 2nd predetermined processing is assigned to the integrated circuit which can be reconfigurated, and an instruction control means writes the 2nd circuitry data in the assigned integrated circuit which can be reconfigurated and makes the integrated circuit which can be reconfigurated perform 2nd predetermined processing While using the parallel computer which can be reconfigurated, being able to assign the 2nd predetermined processing automatically to the integrated circuit which can be reconfigurated and being able to utilize effectively each integrated circuit which can be reconfigurated A user is effective in the ability to use the parallel computer which can be reconfigurated, without being conscious of the integrated circuit to assign and which can be reconfigurated.

[0077] According to this invention, an instruction control means extracts the 1st and 2nd configuration setting tables from a storage means. While an instruction control means extracts the 1st circuitry data from a storage means and a circuitry management tool assigns the 1st predetermined processing to the integrated circuit which can be reconfigurated Hold the operating condition of the integrated circuit which can be reconfigurated and an instruction control means writes the 1st circuitry data in the assigned integrated circuit which can be reconfigurated. It is based on the processing information that make the integrated circuit which can be reconfigurated perform 1st predetermined processing, and 1st predetermined processing is performed to it, from the integrated circuit which can be reconfigurated. An

instruction control means extracts the 2nd circuitry data from a storage means, and a circuitry management tool takes into consideration the operating condition of the integrated circuit which can be reconfigurated currently held. When the 2nd predetermined processing is assigned to the integrated circuit which can be reconfigurated, and an instruction control means writes the 2nd circuitry data in the assigned integrated circuit which can be reconfigurated and makes the integrated circuit which can be reconfigurated perform 2nd predetermined processing While using the parallel computer which can be reconfigurated, being able to assign the 2nd predetermined processing automatically to the integrated circuit which can be reconfigurated and being able to utilize effectively each integrated circuit which can be reconfigurated A user is effective in the ability to use the parallel computer which can be reconfigurated, without being conscious of the integrated circuit to assign and which can be reconfigurated.

[0078] According to this invention, an instruction control means extracts the 1st and 2nd configuration setting tables from a storage means. An instruction control means extracts the 1st circuitry data from a storage means, and a circuitry management tool assigns the 1st predetermined processing to the integrated circuit which can be reconfigurated. An instruction control means writes the 1st circuitry data in the assigned integrated circuit which can be reconfigurated. Make the integrated circuit which can be reconfigurated perform 1st predetermined processing, an instruction control means extracts the 2nd circuitry data from a storage means, and a circuitry management tool takes into consideration the operating condition of the integrated circuit which was notified from the instruction control means and which can be reconfigurated. When the 2nd predetermined processing is assigned to the integrated circuit which can be reconfigurated, and an instruction control means writes the 2nd circuitry data in the assigned integrated circuit which can be reconfigurated and makes the integrated circuit which can be reconfigurated perform 2nd predetermined processing While using the parallel computer which can be reconfigurated, being able to assign the 2nd predetermined processing automatically to the integrated circuit which can be reconfigurated and being able to utilize effectively each integrated circuit which can be reconfigurated A user is effective in the ability to use the parallel computer which can be reconfigurated, without being conscious of the integrated circuit to assign and which can be reconfigurated.

[0079] According to this invention, two or more integrated circuits which can be reconfigurated interconnect. The connection relation of two or more predetermined processings which followed the configuration setting table memorized by the storage means is described. The connection relation of two or more continuous predetermined processings in which own beforehand the data of a configuration of that the instruction control means included interconnect of the integrated circuit which can be reconfigurated, and the circuitry management tool is described by the configuration setting table, It is effective in each integrated circuit which can be reconfigurated being effectively utilizable by assigning two or more continuous predetermined processings to the integrated circuit which can be reconfigurated in consideration of interconnect of the integrated circuit which the instruction control means owns and which can be reconfigurated.

[0080] The connection relation of two or more predetermined processings in which the storage means continued according to this invention, The configuration setting table on which it is between the continuous processings of predetermined [two or more], and the required bit width of face at the time of passing data is described is memorized. The data of a configuration of that the instruction control means contained the bit width of face of interconnect of the integrated circuit which can be reconfigurated are owned beforehand. The required bit width of face at the time of a circuitry management tool being between processings in which two or more continuous predetermined processings described by the configuration setting table continued [continued and it was connection-related] and predetermined [two or more], and passing data, By assigning two or more continuous predetermined processings to the integrated circuit which can be reconfigurated in consideration of the bit width of face of interconnect of the integrated circuit which the instruction control means owns and which can be reconfigurated Even if it is the case where the constraint about I/O with the data width of face between [which can be reconfigurated] integrated circuits, and the exterior is added, the

effectiveness that each integrated circuit which can be reconfigurated is effectively utilizable is acquired.

[0081] The configuration setting table on which the storage means described two or more numbers of implementation of the integrated circuit which performs predetermined processing and its processing, and which can be reconfigurated according to this invention, Memorize the data of the logical circuit for performing predetermined processing, and the data of an I/O circuit, and a circuitry management tool corresponds to two or more numbers of implementation. Predetermined processing is assigned to two or more above-mentioned integrated circuits which can be reconfigurated. An instruction control means It is effective in not creating separately the common logical circuit which writes the same logical circuit in them to the same processing in case a logical circuit and an I/O circuit are written in two or more integrated circuits to which predetermined processing was assigned, and which can be reconfigurated.
[0082] According to this invention, in case a circuitry management tool assigns predetermined processing to the integrated circuit which can be reconfigurated, it is effective in predetermined processing being accelerable by assigning the integrated circuit with the wide bit width of face of interconnect which can be reconfigurated.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the parallel computer which consisted of two or more integrated circuits which can rewrite internal circuitry, and which can be reconfigurated and which can be reconfigurated.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] The high-speed operation engine performance is needed in specific applications, such as digital signal processing, and an image processing, a complicated mathematical operation. In such a case, the general-purpose microprocessor of the operation engine performance is inadequate. Moreover, although sufficient operation engine performance will be obtained if the hardware of dedication, such as a custom-made processor, is used, flexible modification of an algorithm etc. is impossible and the design cycle has the fault that it is long and expensive.
[0003] Integrated circuits which can be reconfigurated, such as FPGA (Field Programmable GateArray) which uses SRAM (Static Random Access Memory) etc. as a storage element, consist of a combinational circuit which consists of AND, OR, etc. on 1 chip, a logical block which can realize a flip-flop etc., and a wiring block which makes connection between these logical blocks hold to storage elements, such as SRAM. Therefore, by giving the data of the storage element of a wiring block from the outside as circuitry data, connection between logical blocks can be made and an internal component circuit can be rewritten any number of times dynamically.
[0004] Therefore, it is possible for the operation engine performance higher than a general-purpose microprocessor to be obtained, and to change an algorithm flexibly, and how to obtain the operation engine performance of the purpose is considered, using integrated circuits which can be reconfigurated, such as FPGA, two or more. The thing as shown below is indicated about the parallel computer using such two or more FPGA.
[0005] drawing 13 -- the Patent Publication Heisei No. 502985 [four to] official report -- "-- the approach using the gate array logic which can be reconfigurated electrically -- and Are drawing showing the configuration of the conventional parallel computer which was indicated by the equipment constituted by this" (following, reference 1), and which can be reconfigurated, and it sets to drawing. 81 is the parallel computer which can be reconfigurated. Two or more logic chips 91-94, a memory module 95, the user setting module 96 and the above-mentioned logic chips 91-94, a memory module 95, and the user setting module 96 It is constituted by the interconnect chip 97 which makes arbitration interconnect. The host computer 82 is controlling the hardware configuration of the parallel computer 81 which can be reconfigurated, and its actuation through a host interface 83 and the configuration system 84.
[0006] The equipment which consists of an integrated circuit of the logic chip 91 of N individual connected mutually - 94 grades which can be reconfigurated as shown in drawing 13 is constituted from reference 1, the logical circuit data which should be carried in the integrated circuit which can be reconfigurated are divided into N individual, these data are assigned to the corresponding gate array which can be reconfigurated, it writes in, and the method of making it operate is indicated.
[0007] Moreover, the equipment which consists of two or more integrated circuits which can be reconfigurated is constituted from "the processing unit, system, and approach" (following, reference 2) of JP,8-286908,A that it can reset freely dynamically, and while performing processing, the approach of writing in the integrated circuit which can be reconfigurated dynamically with the instruction from a program is indicated.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, the configuration setting table which described the number of implementation of the integrated circuit which can be reconfigurated which performs predetermined processing and its processing according to this invention, A storage means by which the circuitry data for performing predetermined processing described by this configuration setting table are memorized, The instruction control means which owns beforehand the data of the configuration of the integrated circuit which can be reconfigurated, and extracts a configuration setting table and circuitry data from a storage means, From an instruction control means, the data, the configuration setting table, and circuitry data of the configuration of the integrated circuit which can be reconfigurated Reception, It has the circuitry management tool which assigns predetermined processing to the integrated circuit which can be reconfigurated. By an instruction control means's writing the circuitry data for performing predetermined processing in the integrated circuit which can be reconfigurated based on the quota result of a circuitry management tool, and making the integrated circuit which can be reconfigurated perform the above-mentioned predetermined processing It is effective in the ability to use the parallel computer which can be reconfigurated, without performing automatically assignment to the integrated circuit of predetermined processing which can be reconfigurated, and a user being conscious of assignment to the integrated circuit which can be reconfigurated.
[0074] When a failure arises in either of the integrated circuits which can be reconfigurated according to this invention An instruction control means detects a failure. A circuitry management tool from an instruction control means The data, the configuration setting table, and circuitry data of the configuration of the integrated circuit including a failure which can be reconfigurated Reception, Except for the integrated circuit which the failure produced and which can be reconfigurated, predetermined processing is newly assigned to the integrated circuit which can be reconfigurated. By an instruction control means's writing the circuitry data for performing predetermined processing in the integrated circuit which can be reconfigurated based on the new quota result of a circuitry management tool, and making the integrated circuit which can be reconfigurated perform the above-mentioned predetermined processing Also when a failure occurs in the integrated circuit which can be reconfigurated, it is effective in each integrated circuit which can be reconfigurated being effectively utilizable.
[0075] According to this invention, when a circuitry management tool gives a logical number to the integrated circuit which can be reconfigurated and assigns predetermined processing to it based on a number, it is effective in the ability to assign predetermined processing easily to the integrated circuit which can be reconfigurated.
[0076] According to this invention, an instruction control means extracts the 1st and 2nd configuration setting tables from a storage means. While an instruction control means extracts the 1st circuitry data from a storage means and a circuitry management tool assigns the 1st predetermined processing to the integrated circuit which can be reconfigurated based on the 1st activation start time described by the 1st configuration setting table Hold the operating condition of the integrated circuit which can be reconfigurated and an instruction control means writes the 1st circuitry data in the assigned above-mentioned integrated circuit which can be reconfigurated. Make the integrated circuit which can be

reconfigurated perform 1st predetermined processing, and it is based at the 2nd activation start time described at the 2nd configuration setting table. An instruction control means extracts the 2nd circuitry data from a storage means, and a circuitry management tool takes into consideration the operating condition of the integrated circuit which can be reconfigurated currently held. When the 2nd predetermined processing is assigned to the integrated circuit which can be reconfigurated, and an instruction control means writes the 2nd circuitry data in the assigned integrated circuit which can be reconfigurated and makes the integrated circuit which can be reconfigurated perform 2nd predetermined processing While using the parallel computer which can be reconfigurated, being able to assign the 2nd predetermined processing automatically to the integrated circuit which can be reconfigurated and being able to utilize effectively each integrated circuit which can be reconfigurated A user is effective in the ability to use the parallel computer which can be reconfigurated, without being conscious of the integrated circuit to assign and which can be reconfigurated.

[0077] According to this invention, an instruction control means extracts the 1st and 2nd configuration setting tables from a storage means. While an instruction control means extracts the 1st circuitry data from a storage means and a circuitry management tool assigns the 1st predetermined processing to the integrated circuit which can be reconfigurated Hold the operating condition of the integrated circuit which can be reconfigurated and an instruction control means writes the 1st circuitry data in the assigned integrated circuit which can be reconfigurated. It is based on the processing information that make the integrated circuit which can be reconfigurated perform 1st predetermined processing, and 1st predetermined processing is performed to it, from the integrated circuit which can be reconfigurated. An instruction control means extracts the 2nd circuitry data from a storage means, and a circuitry management tool takes into consideration the operating condition of the integrated circuit which can be reconfigurated currently held. When the 2nd predetermined processing is assigned to the integrated circuit which can be reconfigurated, and an instruction control means writes the 2nd circuitry data in the assigned integrated circuit which can be reconfigurated and makes the integrated circuit which can be reconfigurated perform 2nd predetermined processing While using the parallel computer which can be reconfigurated, being able to assign the 2nd predetermined processing automatically to the integrated circuit which can be reconfigurated and being able to utilize effectively each integrated circuit which can be reconfigurated A user is effective in the ability to use the parallel computer which can be reconfigurated, without being conscious of the integrated circuit to assign and which can be reconfigurated.

[0078] According to this invention, an instruction control means extracts the 1st and 2nd configuration setting tables from a storage means. An instruction control means extracts the 1st circuitry data from a storage means, and a circuitry management tool assigns the 1st predetermined processing to the integrated circuit which can be reconfigurated. An instruction control means writes the 1st circuitry data in the assigned integrated circuit which can be reconfigurated. Make the integrated circuit which can be reconfigurated perform 1st predetermined processing, an instruction control means extracts the 2nd circuitry data from a storage means, and a circuitry management tool takes into consideration the operating condition of the integrated circuit which was notified from the instruction control means and which can be reconfigurated. When the 2nd predetermined processing is assigned to the integrated circuit which can be reconfigurated, and an instruction control means writes the 2nd circuitry data in the assigned integrated circuit which can be reconfigurated and makes the integrated circuit which can be reconfigurated perform 2nd predetermined processing While using the parallel computer which can be reconfigurated, being able to assign the 2nd predetermined processing automatically to the integrated circuit which can be reconfigurated and being able to utilize effectively each integrated circuit which can be reconfigurated A user is effective in the ability to use the parallel computer which can be reconfigurated, without being conscious of the integrated circuit to assign and which can be reconfigurated.

[0079] According to this invention, two or more integrated circuits which can be reconfigurated interconnect. The connection relation of two or more predetermined processings which followed the configuration setting table memorized by the storage means is described. The connection relation of two

or more continuous predetermined processings in which own beforehand the data of a configuration of that the instruction control means included interconnect of the integrated circuit which can be reconfigurated, and the circuitry management tool is described by the configuration setting table, It is effective in each integrated circuit which can be reconfigurated being effectively utilizable by assigning two or more continuous predetermined processings to the integrated circuit which can be reconfigurated in consideration of interconnect of the integrated circuit which the instruction control means owns and which can be reconfigurated.

[0080] The connection relation of two or more predetermined processings in which the storage means continued according to this invention, The configuration setting table on which it is between the continuous processings of predetermined [two or more], and the required bit width of face at the time of passing data is described is memorized. The data of a configuration of that the instruction control means contained the bit width of face of interconnect of the integrated circuit which can be reconfigurated are owned beforehand. The required bit width of face at the time of a circuitry management tool being between processings in which two or more continuous predetermined processings described by the configuration setting table continued [continued and it was connection-related] and predetermined [two or more], and passing data, By assigning two or more continuous predetermined processings to the integrated circuit which can be reconfigurated in consideration of the bit width of face of interconnect of the integrated circuit which the instruction control means owns and which can be reconfigurated Even if it is the case where the constraint about I/O with the data width of face between [which can be reconfigurated] integrated circuits, and the exterior is added, the effectiveness that each integrated circuit which can be reconfigurated is effectively utilizable is acquired.

[0081] The configuration setting table on which the storage means described two or more numbers of implementation of the integrated circuit which performs predetermined processing and its processing, and which can be reconfigurated according to this invention, Memorize the data of the logical circuit for performing predetermined processing, and the data of an I/O circuit, and a circuitry management tool corresponds to two or more numbers of implementation. Predetermined processing is assigned to two or more above-mentioned integrated circuits which can be reconfigurated. An instruction control means It is effective in not creating separately the common logical circuit which writes the same logical circuit in them to the same processing in case a logical circuit and an I/O circuit are written in two or more integrated circuits to which predetermined processing was assigned, and which can be reconfigurated.

[0082] According to this invention, in case a circuitry management tool assigns predetermined processing to the integrated circuit which can be reconfigurated, it is effective in predetermined processing being accelerable by assigning the integrated circuit with the wide bit width of face of interconnect which can be reconfigurated.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Since the conventional parallel computer which can be reconfigurated is constituted as mentioned above, one processing and operation which are expressed in a digital logic network With the technique of the above-mentioned reference 1 supplied to two or more integrated circuits which can be reconfigurated When two or more different processings were performed to coincidence and these processings were supplied to two or more integrated circuits which can be reconfigurated, directions had to be given for every processing and the same or the technical problem that assignment could not be determined automatically occurred.
[0009] Moreover, circuitry data were divided into N individual and the technical problem that could divide data and they could not necessarily be assigned to N individual depending on circuitry data and the connection configuration between [which can be reconfigurated] integrated circuits occurred with the technique of the above-mentioned reference 1 which assigns those data to each integrated circuit which can be reconfigurated.
[0010] Furthermore, when adding and performing processing which is further different while performing two or more processings by assignment from a program with the technique of the above-mentioned reference 2 change dynamically the circuitry of the integrated circuit which can be reconfigurated, in order to assign processing to the integrated circuit which is not used and which can be reconfigurated, a certain assignment by the user was needed, and the technical problem that the integrated circuit which can be reconfigurated cannot be used efficiently was.
[0011] This invention was made in order to solve the above technical problems, and while performing automatically assignment to the integrated circuit of two or more different processings which can be reconfigurated, it carries out dynamically according to the connection configuration and the operating condition between [which can be reconfigurated] integrated circuits, and it aims at the same or obtaining the parallel computer which utilizes effectively each integrated circuit which can be reconfigurated and which can be reconfigurated in the equipment which consisted of two or more integrated circuits which can be reconfigurated.
[0012] Moreover, it aims at obtaining the parallel computer which enables use of equipment and which can be reconfigurated, without a user being conscious of assignment to the integrated circuit which can be reconfigurated.

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MEANS

[Means for Solving the Problem] In what consisted of two or more integrated circuits with which the parallel computer concerning this invention which can be reconfigurated can rewrite internal circuitry, and which can be reconfigurated The configuration setting table which described the number of implementation of the above-mentioned integrated circuit which performs predetermined processing and its processing, and which can be reconfigurated, A storage means by which the circuitry data for performing the above-mentioned predetermined processing described by this configuration setting table are memorized, The instruction control means which owns beforehand the data of the configuration of the above-mentioned integrated circuit which can be reconfigurated, and extracts the above-mentioned configuration setting table and the above-mentioned circuitry data from the above-mentioned storage means, From the above-mentioned instruction control means, the data, the above-mentioned configuration setting table, and the above-mentioned circuitry data of the configuration of the above-mentioned integrated circuit which can be reconfigurated Reception, It has the circuitry management tool which assigns the above-mentioned predetermined processing to the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means writes the circuitry data for performing the above-mentioned predetermined processing in the above-mentioned integrated circuit which can be reconfigurated based on the quota result of the above-mentioned circuitry management tool, and the above-mentioned integrated circuit which can be reconfigurated is made to perform the above-mentioned predetermined processing.
[0014] When a failure arises in either of the integrated circuits which can be reconfigurated, the parallel computer concerning this invention which can be reconfigurated An instruction control means detects the above-mentioned failure. A circuitry management tool from the above-mentioned instruction control means The data, the configuration setting table, and circuitry data of the configuration of the integrated circuit including the above-mentioned failure which can be reconfigurated Reception, Except for the integrated circuit which the above-mentioned failure produced and which can be reconfigurated, predetermined processing is newly assigned to the integrated circuit which can be reconfigurated. The above-mentioned instruction control means writes the circuitry data for performing the above-mentioned predetermined processing in the above-mentioned integrated circuit which can be reconfigurated based on the new quota result of the above-mentioned circuitry management tool, and the above-mentioned integrated circuit which can be reconfigurated is made to perform the above-mentioned predetermined processing.
[0015] The parallel computer concerning this invention which can be reconfigurated gives a number with a circuitry management tool logical to the integrated circuit which can be reconfigurated, and predetermined processing is assigned based on the above-mentioned number.
[0016] The 1st configuration setting table on which the number of implementation of the integrated circuit with which, as for the parallel computer concerning this invention which can be reconfigurated, a storage means performs 1st predetermined processing and predetermined processing of the above 1st, and which can be reconfigurated, and the 1st activation start time were described, The 2nd configuration setting table on which the number of implementation of the above-mentioned integrated circuit which

performs the 1st circuitry data for performing predetermined processing of the above 1st, 2nd predetermined processing, and predetermined processing of the above 2nd, and which can be reconfigurated, and the 2nd activation start time were described, The 2nd circuitry data for performing predetermined processing of the above 2nd is memorized. An instruction control means extracts the above 1st and the 2nd configuration setting table from the above-mentioned storage means. It is based at the 1st activation start time described by the configuration setting table of the above 1st. While the above-mentioned instruction control means extracts the circuitry data of the above 1st from the above-mentioned storage means and a circuitry management tool assigns predetermined processing of the above 1st to the above-mentioned integrated circuit which can be reconfigurated The operating condition of the above-mentioned integrated circuit which can be reconfigurated is held. The above-mentioned instruction control means The circuitry data of the above 1st are written in the assigned above-mentioned integrated circuit which can be reconfigurated. Make the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 1st, and it is based at the 2nd activation start time described at the configuration setting table of the above 2nd. The above-mentioned instruction control means extracts the circuitry data of the above 2nd from the above-mentioned storage means, and the above-mentioned circuitry management tool takes into consideration the operating condition of the above-mentioned integrated circuit which can be reconfigurated currently held. Predetermined processing of the above 2nd is assigned to the above-mentioned integrated circuit which can be reconfigurated, and the above-mentioned instruction control means writes the circuitry data of the above 2nd in the assigned above-mentioned integrated circuit which can be reconfigurated, and makes the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 2nd.

[0017] The 1st configuration setting table on which the number of implementation of the integrated circuit with which, as for the parallel computer concerning this invention which can be reconfigurated, a storage means performs 1st predetermined processing and predetermined processing of the above 1st, and which can be reconfigurated was described, The 2nd configuration setting table on which the number of implementation of the above-mentioned integrated circuit which performs 2nd predetermined processing and predetermined processing of the above 2nd, and which can be reconfigurated was described to be the 1st circuitry data for performing predetermined processing of the above 1st, The 2nd circuitry data for performing predetermined processing of the above 2nd is memorized. An instruction control means extracts the above 1st and the 2nd configuration setting table from the above-mentioned storage means. While the above-mentioned instruction control means extracts the circuitry data of the above 1st from the above-mentioned storage means and a circuitry management tool assigns predetermined processing of the above 1st to the above-mentioned integrated circuit which can be reconfigurated The operating condition of the above-mentioned integrated circuit which can be reconfigurated is held. The above-mentioned instruction control means The circuitry data of the above 1st are written in the assigned above-mentioned integrated circuit which can be reconfigurated. It is based on the processing information that make the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 1st, and predetermined processing of the above 1st is performed to it, from the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means extracts the circuitry data of the above 2nd from the above-mentioned storage means, and the above-mentioned circuitry management tool takes into consideration the operating condition of the above-mentioned integrated circuit which can be reconfigurated currently held. Predetermined processing of the above 2nd is assigned to the above-mentioned integrated circuit which can be reconfigurated, and the above-mentioned instruction control means writes the circuitry data of the above 2nd in the assigned above-mentioned integrated circuit which can be reconfigurated, and makes the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 2nd.

[0018] The 1st configuration setting table on which the number of implementation of the integrated circuit with which, as for the parallel computer concerning this invention which can be reconfigurated, a storage means performs 1st predetermined processing and predetermined processing of the above 1st,

and which can be reconfigurated was described, The 2nd configuration setting table on which the number of implementation of the above-mentioned integrated circuit which performs 2nd predetermined processing and predetermined processing of the above 2nd, and which can be reconfigurated was described to be the 1st circuitry data for performing predetermined processing of the above 1st, The 2nd circuitry data for performing predetermined processing of the above 2nd is memorized. An instruction control means extracts the above 1st and the 2nd configuration setting table from the above-mentioned storage means. The above-mentioned instruction control means extracts the circuitry data of the above 1st from the above-mentioned storage means. A circuitry management tool assigns predetermined processing of the above 1st to the above-mentioned integrated circuit which can be reconfigurated. The above-mentioned instruction control means writes the circuitry data of the above 1st in the assigned above-mentioned integrated circuit which can be reconfigurated. Make the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 1st, and the above-mentioned instruction control means extracts the circuitry data of the above 2nd from the above-mentioned storage means to it. The above-mentioned circuitry management tool takes into consideration the operating condition of the above-mentioned integrated circuit which can be reconfigurated notified from the above-mentioned instruction control means. Predetermined processing of the above 2nd is assigned to the above-mentioned integrated circuit which can be reconfigurated, and the above-mentioned instruction control means writes the circuitry data of the above 2nd in the assigned above-mentioned integrated circuit which can be reconfigurated, and makes the above-mentioned integrated circuit which can be reconfigurated perform predetermined processing of the above 2nd.

[0019] As for the parallel computer concerning this invention which can be reconfigurated, two or more integrated circuits which can be reconfigurated interconnect. The connection relation of two or more predetermined processings which followed the configuration setting table memorized by the storage means is described. The connection relation of two or more continuous predetermined processings in which own beforehand the data of a configuration of that the instruction control means included the above-mentioned interconnect of the above-mentioned integrated circuit which can be reconfigurated, and the circuitry management tool is described by the above-mentioned configuration setting table, In consideration of the above-mentioned interconnect of the above-mentioned integrated circuit which the above-mentioned instruction control means owns and which can be reconfigurated, two or more predetermined processings which carried out [above-mentioned] continuation are assigned to the above-mentioned integrated circuit which can be reconfigurated.

[0020] The connection relation of two or more predetermined processings in which, as for the parallel computer concerning this invention which can be reconfigurated, the storage means continued, The configuration setting table on which it is between the processings which carried out [above-mentioned] continuation of predetermined [two or more], and the required bit width of face at the time of passing data is described is memorized. The data of a configuration of that the instruction control means contained the bit width of face of interconnect of the integrated circuit which can be reconfigurated are owned beforehand. The required bit width of face at the time of a circuitry management tool being between the processings in which two or more continuous predetermined processings described by the above-mentioned configuration setting table carried out connection relation and the above-mentioned continuation of predetermined [two or more], and passing data, In consideration of the bit width of face of the above-mentioned interconnect of the above-mentioned integrated circuit which the above-mentioned instruction control means owns and which can be reconfigurated, two or more predetermined processings which carried out [above-mentioned] continuation are assigned to the above-mentioned integrated circuit which can be reconfigurated.

[0021] The configuration setting table on which, as for the parallel computer concerning this invention which can be reconfigurated, the storage means described two or more numbers of implementation of the integrated circuit which performs predetermined processing and its processing, and which can be reconfigurated, Memorize the data of the logical circuit for performing the above-mentioned predetermined processing, and the data of an I/O circuit, and a circuitry management tool corresponds to two or more above-mentioned numbers of implementation. The above-mentioned predetermined

processing is assigned to two or more above-mentioned integrated circuits which can be reconfigurated, and in case an instruction control means writes the above-mentioned logical circuit and the above-mentioned I/O circuit in two or more integrated circuits to which the above-mentioned predetermined processing was assigned and which can be reconfigurated, the same logical circuit is written in to the same processing.

[0022] The parallel computer concerning this invention which can be reconfigurated is assigned to the above-mentioned integrated circuit with the wide bit width of face of interconnect which can be reconfigurated in case a circuitry management tool assigns predetermined processing to the integrated circuit which can be reconfigurated.

[0023]

[Embodiment of the Invention] Hereafter, one gestalt of implementation of this invention is explained. Gestalt 1. drawing 1 of operation is drawing showing the configuration of the parallel computer by the gestalt 1 of implementation of this invention which can be reconfigurated. In drawing 1 , 1 is an instruction control means which the parallel computer which can be reconfigurated, and 11-18 give the integrated circuit (FPGA) of plurality (eight [in this case,]) which can be reconfigurated to the integrated circuits 11-18 which can be reconfigurated, and 2 gives control instruction and data, and controls actuation, and 100 is a bus signal line which performs communication link actuation which includes data transfer and circuit information transfer between the integrated circuits 11-18 which can be reconfigurated, and the instruction control means 2.

[0024] Moreover, in drawing 1 , 4 is a storage means by which the configuration setting table which described the number of the integrated circuits which perform predetermined processing and its processing, and which can be reconfigurated (the number of implementation), and the circuitry data for performing predetermined processing described by this configuration setting table are memorized. Drawing 2 is drawing showing the configuration setting table 51, and the number of the integrated circuits which perform predetermined processing and its processing and which can be reconfigurated (the number of implementation) is described. Moreover, the circuitry data memorized by the storage means 4 are wiring connection data between the logical blocks inside a certain integrated circuit which can be reconfigurated, and the predetermined circuit which performs predetermined processing to those integrated circuits 11-18 that can be reconfigurated is realized by writing this circuitry data in the integrated circuits 11-18 which can be reconfigurated.

[0025] Furthermore, in drawing 1 , 3 is a circuitry management tool which determines the suitable assignment to the integrated circuits 11-18 of reception and predetermined processing of the configuration setting table and circuitry data which are memorized by the storage means 4, and the data of the configuration of the integrated circuit 11-18 which the instruction control means 2 owns beforehand, and which can be reconfigurated which can be reconfigurated. 111 is a signal line which delivers the information memorized by the storage means 4 to the instruction control means 2.

[0026] Next, actuation is explained. First, the instruction control means 2 extracts the configuration setting table 51 shown in drawing 2 from the storage means 4 at the time of starting of this parallel computer 1 that can be reconfigurated. Next, the instruction control means 2 extracts the circuitry data for performing each predetermined processing described by the configuration setting table 51 from the storage means 4.

[0027] Then, the circuitry management tool 3 determines reception and everywhere assignment to the integrated circuits 11-18 of processing of a law which can be reconfigurated from the instruction control means 2 for the configuration setting table 51 extracted from the storage means 4, circuitry data, and the data of the configuration of the integrated circuit 11-18 which the instruction control means 2 owns beforehand and which can be reconfigurated. The instruction control means 2 writes the circuitry data for [which the circuitry management tool 3 determined] assigning and performing each predetermined processing based on a result in each integrated circuits 11-18 which can be reconfigurated.

[0028] After the writing of the circuitry data to each integrated circuits 11-18 which can be reconfigurated is performed, the instruction control means 2 supplies suitable data and a clock of operation, and makes each integrated circuits 11-18 which can be reconfigurated perform predetermined

processing to the integrated circuits 11-18 to which predetermined processing was assigned and which can be reconfigurated based on the quota result of the circuitry management tool 3.
[0029] Thus, when the circuitry management tool 3 assigns predetermined processing to the suitable integrated circuits 11-18 which can be reconfigurated in consideration of the configuration of the integrated circuits 11-18 which can be reconfigurated and the instruction control means 2 writes in the integrated circuits 11-18 which can be reconfigurated for the circuitry data for performing predetermined processing, the parallel computer which performs predetermined processing and which can be reconfigurated is realized automatically.
[0030] Although the above-mentioned example is an example at the time of starting of the parallel computer 1 which can be reconfigurated Moreover, the circuit to realize is changed after starting the parallel computer 1 which can be reconfigurated. By preparing another configuration setting table and circuitry data, and performing the same procedure as the time of starting of the parallel computer 1 which can be reconfigurated, when making another predetermined processing perform The circuitry data for performing assignment of another predetermined processing and another predetermined processing are again written in to each integrated circuits 11-18 which can be reconfigurated. Thereby, after starting can write in the circuitry data to each integrated circuits 11-18 which can be reconfigurated.
[0031] Moreover, after the time of starting, or starting, when a failure arises in either of the integrated circuits 11-18 which can be reconfigurated, the instruction control means 2 detects this failure, and should just perform assignment of predetermined processing, and the writing of circuitry data in the above-mentioned procedure again. The writing to the integrated circuits 11-18 of circuitry data which can be reconfigurated can be performed without being influenced by this, according to the failure of the integrated circuits 11-18 which can be reconfigurated etc., even if it is the case where modification arises in a configuration.
[0032] For example, in the case of the configuration setting table 51 shown in drawing 2 , it is the example which realizes predetermined processing 61 with five integrated circuits which can be reconfigurated, and realizes predetermined processing 62 with two integrated circuits which can be reconfigurated, and as long as this condition is fulfilled, the circuitry management tool 3 determines assignment freely. As an example of the technique of assignment, the circuitry management tool 3 gives a logical number to the integrated circuits 11-18 which can be reconfigurated, and can consider how to assign predetermined processing to order with a small number. By this technique, when realizing with the configuration of the parallel computer 1 which shows the configuration setting table 51 shown in drawing 2 to drawing 1 and which can be reconfigurated, the predetermined processing 61 is assigned to the integrated circuits 11-15 which can be reconfigurated, the predetermined processing 62 is assigned to the integrated circuits 16 and 17 which can be reconfigurated, and the circuitry data which correspond, respectively are written in.
[0033] Moreover, for example, when a failure occurs in the integrated circuit 14 which can be reconfigurated, the circuitry management tool 3 assigns the predetermined processing 61 to the integrated circuits 11-13 which can be reconfigurated, and 15 and 16 except for the integrated circuit 14 which can be reconfigurated, the predetermined processing 62 is assigned to the integrated circuits 17 and 18 which can be reconfigurated, and the instruction control means 2 writes in the circuitry data which correspond, respectively.
[0034] As mentioned above, the effectiveness that the parallel computer which can be reconfigurated can be used is acquired, without a user being conscious of assignment to the integrated circuit which can be reconfigurated by the circuitry management tool's 3 assigning two or more same or different predetermined processings automatically to the integrated circuit which can be reconfigurated, and writing in the circuitry data for performing predetermined processing to each integrated circuits 11-18 which can be reconfigurated, respectively according to the gestalt 1 of this operation.
[0035] Moreover, the effectiveness that each integrated circuits 11-18 which can be reconfigurated are effectively utilizable is acquired by changing the circuit to realize, and performing the same assignment and the same writing, when making another predetermined processing perform, or also when a failure occurs in the integrated circuits 11-18 which can be reconfigurated after starting the parallel computer 1

which can be reconfigurated.
[0036] gestalt 2. of operation -- at the time of use of the parallel computer 1 which can be reconfigurated, the gestalt 2 of implementation of this invention adds circuitry data, and is realized. Drawing 3 and drawing 4 are drawings showing the configuration setting tables 52 and 53 which described the number of implementation which realizes predetermined processings and those processings, and the activation start time which starts activation of a configuration setting table is described by each configuration setting tables 52 and 53. From this activation start time, it shall assign and writing and predetermined processing shall be performed.
[0037] The configuration of the parallel computer 1 in the gestalt 2 of this operation which can be reconfigurated is the same as the configuration shown in drawing 1 of the gestalt 1 of operation, and the circuitry data for carrying out predetermined processings 63-65 described by the configuration setting tables 52 and 53 and the configuration setting table to the storage means 4 are memorized.
[0038] Next, actuation is explained. First, the instruction control means 2 extracts the configuration setting tables 52 and 53 from the storage means 4 at the time of starting of this parallel computer 1 that can be reconfigurated. Since the activation start time described by the configuration setting table 52 is 0, it sets to time amount 0. Next, the instruction control means 2 The circuitry data for performing predetermined processings 63 and 64 described by the configuration setting table 52 shown in drawing 3 are extracted from the storage means 4, by the same procedure as the gestalt 1 of operation, assignment of predetermined processing and the writing of circuitry data are performed, and processing of a law is performed everywhere. And in case the instruction control means 2 writes in, the circuitry management tool 3 holds the operating condition of each integrated circuits 11-18 which can be reconfigurated.
[0039] Next, since the activation start time described by the configuration setting table 53 is 100, in time amount 100, the instruction control means 2 extracts the circuitry data for performing predetermined processing 65 described by the configuration setting table 53 shown in drawing 4 from the storage means 4. Then, the circuitry management tool 3 assigns the predetermined processing 65 to the integrated circuits 11-18 which are not using the circuitry data for performing the configuration setting table 53 and predetermined processing 65 from the instruction control means 2 in consideration of the operating condition of reception and each integrated circuits 11-18 which are held, and which can be reconfigurated and which can be reconfigurated. The instruction control means 2 writes in the circuitry data only corresponding to the integrated circuits 11-18 with which assignment was performed and which can be reconfigurated based on the quota result of the circuitry management tool 3. After writing is performed, each predetermined processing is performed.
[0040] Moreover, activation initiation of each configuration setting tables 52 and 53 may specify it that activation initiation of each configuration setting table is performed by some conditions rather than may specify time amount. For example, in the above-mentioned example, the configuration of the configuration setting table 52 is realized and suppose that predetermined processings 63 and 64 were performed. In this case, when the predetermined processing 63 is completed, the instruction control means 2 may be made to realize the contents which extract that information from the storage means 4, and are described [information] by the configuration setting table 53 in reception and the configuration setting table 53. Moreover, for example, the signal of the processing termination from one of the integrated circuits 11-18 which can be reconfigurated may be specified that activation initiation of a configuration setting table is performed a condition [what the instruction control means 2 receives].
[0041] Moreover, you may make it start activation of each configuration setting tables 52 and 53 according to specific time amount, or not conditions but the operating condition of the integrated circuits 11-18 which can be reconfigurated. The configuration setting table 52 shown in the configuration setting table 54 shown in drawing 5 instead of and drawing 3 is memorized to the storage means 4, and drawing 5 performs the configuration setting table 54 after the configuration setting table 52. [the configuration setting table 53 which is drawing showing the configuration setting table 54, and is shown in above-mentioned drawing 4]
[0042] In this case, the processing 63 predetermined by time amount 0 is assigned to three pieces, the predetermined processing 64 is assigned to two pieces and the integrated circuits 11-18 which can be

reconfigurated, and it performs. Next, since the activation start time described by the configuration setting table 54 is 1, by time amount 1, the configuration setting table 54 is performed and the predetermined processing 66 is assigned to five pieces and the integrated circuits 11-18 which can be reconfigurated. However, since there are only three intact integrated circuits 11-18 which can be reconfigurated when the processing 63 predetermined in this time or 64 is not completed, the predetermined processing 66 cannot be assigned.

[0043] In this case, activation of the configuration setting table 54 is interrupted by the circuitry management tool 3. Then, termination of predetermined processing 63 or the predetermined, predetermined processing 64 sends the information about the operating condition of the integrated circuits 11-18 which can be reconfigurated from the instruction control means 2 to the circuitry management tool 3. Since the number of the intact integrated circuits 11-18 which can be reconfigurated becomes five or more about the operating condition of the integrated circuits 11-18 which are held with the circuitry management tool 3 and which can be reconfigurated at this time, by the circuitry management tool 3, activation of the configuration setting table 54 is resumed and assignment is performed.

[0044] The writing to the integrated circuits 11-18 of the circuitry data corresponding to the operating condition of the integrated circuits 11-18 which can be reconfigurated etc. which can be reconfigurated can be performed by this, the integrated circuits 11-18 which can be reconfigurated can be used effectively, and a user can use the parallel computer which can be reconfigurated, without being conscious of the integrated circuits 11-18 to assign and which can be reconfigurated.

[0045] While using the parallel computer which can be reconfigurated, according to the gestalt 2 of this operation, the circuitry management tool 3 as mentioned above, according to predetermined time amount and predetermined conditions Moreover, when predetermined processing is assigned to the suitable integrated circuits 11-18 which can be reconfigurated and the instruction control means 2 writes in circuitry data according to the operating condition of the integrated circuits 11-18 which can be reconfigurated While being able to assign predetermined processing automatically to the integrated circuits 11-18 which can be reconfigurated and being able to utilize effectively each integrated circuits 11-18 which can be reconfigurated, a user The effectiveness which can use the parallel computer which can be reconfigurated and to say is acquired without being conscious of the integrated circuits 11-18 to assign and which can be reconfigurated.

[0046] Gestalt 3. drawing 6 of operation is drawing showing the configuration of the parallel computer by the gestalt 3 of implementation of this invention which can be reconfigurated. As shown in drawing, between [of specification / which can be reconfigurated] integrated circuits 11-18 is connected, and one arithmetic circuit consists of combining two or more circuitry data. In drawing 6 , the parallel computer 1 which can be reconfigurated has two or more of the same integrated circuits 11-18 as drawing 1 of the gestalt 1 of operation which can be reconfigurated, the instruction control means 2, the circuitry management tool 3, the storage means 4, and a signal line 100,111. Moreover, in drawing 6 , communication link actuation including data transfer is performed through signal lines 101-110 the integrated circuit 11 which can be reconfigurated - between 18.

[0047] Drawing 7 is drawing showing the configuration setting table 55 which described the number of implementation which realizes a series of predetermined processings and those processings, and the circuitry data for carrying out predetermined processings 67, 68, 69, 70, and 71 described by this configuration setting table 55 and the configuration setting table 55 to the storage means 4 are memorized.

[0048] Next, actuation is explained. First, the instruction control means 2 extracts the configuration setting table 55 shown in drawing 7 from the storage means 4 at the time of starting of this parallel computer 1 that can be reconfigurated. Next, the instruction control means 2 extracts the circuitry data for performing each predetermined processing described by the configuration setting table 55 from the storage means 4. Then, the circuitry management tool 3 determines everywhere assignment to the integrated circuits 11-18 of processing of a law which can be reconfigurated from the instruction control means 2 based on reception and those information for the configuration setting table 55, circuitry data,

the data of the configuration of the integrated circuit 11-18 which the instruction control means 2 owns beforehand and which can be reconfigurated, and the information on connection of each mutual. Subsequent processing is the same as the case of the gestalt 1 of operation.
[0049] For example, after inputting and performing the data from the instruction control means 2 to the predetermined processing 67 in the case of drawing 7 , The output is passed and performed to the predetermined processing 68 and the predetermined processing 69. The output of the predetermined processings 68 and 69 It is the example which passes and performs to the predetermined processing 70, realizes continuous processing in which an output is passed to the instruction control means 2, with the one-set integrated circuit which can be reconfigurated, and realizes predetermined processing 71 with three integrated circuits which can be reconfigurated.
[0050] The circuitry management tool 3 divides and hits the integrated circuits 11-18 which can be reconfigurated in each circuitry data for performing predetermined processings 67-71 under the connection-related constraint of the predetermined processings 67-70, the constraint which assigns one set of configurations which the predetermined processings 67-70 followed, and the constraint of assigning three predetermined processings 71. As an example, the predetermined processing 67 to the integrated circuit 11 which can be reconfigurated the predetermined processing 68 to the integrated circuit 12 which can be reconfigurated The integrated circuit 13 which can be reconfigurated, and the predetermined processing 71 to 14 and 17 the predetermined processing 69 to the integrated circuit 15 which can be reconfigurated Assignment which fulfilled the above-mentioned constraint can be performed by distributing predetermined processing so that it may say that the predetermined processing 70 is assigned to the integrated circuit 16 which can be reconfigurated, and predetermined processing is not assigned to the integrated circuit 18 which can be reconfigurated.
[0051] the activity which assigns circuitry data to the integrated circuits 11-18 which can be reconfigurated based on such conditions -- mathematical -- "-- conditional -- it is formulized as maximum minimum problem." About the solution method of such a problem, much technique is proposed from the former and which technique may be used at the quota process of this invention. Thereby, by combining two or more circuitry data, when one arithmetic circuit is realized, in consideration of connection between [which can be reconfigurated] integrated circuits 11-18, circuitry data can be written in the suitable integrated circuits 11-18 which can be reconfigurated.
[0052] According to the gestalt 3 of this operation, by as mentioned above, the thing for which two or more circuitry data are combined When one arithmetic circuit is realized, the circuitry management tool 3 determines assignment of predetermined processing in consideration of connection between [which can be reconfigurated] integrated circuits 11-18. When the instruction control means 2 writes circuitry data in the suitable integrated circuits 11-18 which can be reconfigurated, the effectiveness that each integrated circuits 11-18 which can be reconfigurated are effectively utilizable is acquired.
[0053] It is drawing showing the configuration of the parallel computer which can be reconfigurated according [gestalt 4. drawing 8 of operation] to the gestalt 4 of implementation of this invention, and as shown in drawing, between [of specification / which can be reconfigurated] integrated circuits 11-18 is connected, and the connection configuration to the exterior of the signal line in the integrated circuits 11-18 which can be reconfigurated changes with each integrated circuits 11-18 which can be reconfigurated. In drawing 8 , the parallel computer 1 which can be reconfigurated has two or more integrated circuits 11-18 which can be reconfigurated, instruction control means 2, circuitry management tools 3, and storage means 4 like drawing 6 of the gestalt 3 of operation. The integrated circuits 11-18 which can be reconfigurated perform communication link actuation including data transfer and circuit information transfer through the instruction control means 2 and a signal line 200. Moreover, the integrated circuit 11 which can be reconfigurated - between 18, communication link actuation including data transfer and circuit information transfer is performed through signal lines 201-210.
[0054] Moreover, signal lines 201-203,205,206,209 shall be eight pins for data I/O, and the signal line 204,207,208,210 shall consist of 16 pins for data I/O. For this reason, signal lines 201-203,205,206,209 are signal lines of 8-bit width of face, and a signal line 204,207,208,210 is considered to be the signal

line of 16-bit width of face.
[0055] In case drawing 9 passes data by processing of a law the number of implementation, and everywhere which realizes a series of predetermined processings and those processings, it is drawing showing the configuration setting table 56 which described required bit width of face. The circuitry data for carrying out predetermined processings 72-75 described by the configuration setting table 56 and the configuration setting table 56 to the storage means 4 are memorized.
[0056] Next, actuation is explained. First, the instruction control means 2 extracts the configuration setting table 56 from the storage means 4 at the time of starting of this parallel computer 1 that can be reconfigurated. Next, the instruction control means 2 extracts the circuitry data for performing each predetermined processing described on the configuration setting table 56 from the storage means 4. Then, the circuitry management tool 3 determines everywhere assignment to the integrated circuits 11-18 of processing of a law which can be reconfigurated from the instruction control means 2 based on reception and those received information for the information on the data width of face of the configuration setting table 56, circuitry data, and the connection relation between [which can be reconfigurated] integrated circuits 11-18 and each signal line that the instruction control means 2 owns beforehand. Subsequent processing is the same as the case of the gestalt 1 of operation.
[0057] Thereby, when the connection configuration to the exterior of the signal line in the integrated circuits 11-18 which can be reconfigurated changes with each integrated circuits 11-18 which can be reconfigurated, in consideration of the data width of face of a signal line, circuitry data can be written in the suitable integrated circuit which can be reconfigurated.
[0058] For example, in the case of drawing 9 , it is the example which realizes continuous processing in which sequential execution activation of the predetermined processings 72-75 is carried out, with two pieces and the integrated circuit which can be reconfigurated. Moreover, in order to pass data to the predetermined processings 72-73 and the predetermined processings 73-74, the signal line of 16-bit width of face is required, and in order to pass data to the predetermined processings 74-75, the signal line of 8-bit width of face is needed. Moreover, from the instruction control means 2, the predetermined processing 72 must output reception to the instruction control means 2, and the predetermined processing 75 must output the data of a processing result for data.
[0059] Assignment which fulfilled the above-mentioned constraint can be performed by distributing predetermined processing as the predetermined processing 73 is assigned as an example to the integrated circuits 11 and 14 which can be reconfigurated for the predetermined processing 72 at the integrated circuits 15 and 18 which can be reconfigurated and the predetermined processing 75 is assigned to the integrated circuits 16 and 17 which can be reconfigurated for the predetermined processing 74 at the integrated circuits 12 and 13 which can be reconfigurated. Even if it is the case where the constraint about I/O with such data width of face and the exterior is added, the technique of assigning predetermined processing to the integrated circuits 11-18 which can be reconfigurated is the same as the gestalt 3 of operation, and good.
[0060] As mentioned above, even if it is the case where the constraint about I/O with the data width of face between [which can be reconfigurated] integrated circuits 11-18, and the exterior is added according to the gestalt 4 of this operation The circuitry management tool 3 by determining assignment of predetermined processing and writing circuitry data in the suitable integrated circuits [the instruction control means 2] 11-18 which can be reconfigurated in consideration of connection between [which can be reconfigurated] integrated circuits 11-18, and data width of face The effectiveness that each integrated circuits 11-18 which can be reconfigurated are effectively utilizable is acquired.
[0061] gestalt 5. of operation -- the configuration of the parallel computer 1 in the gestalt of this operation which can be reconfigurated is the same as drawing 8 of the gestalt 4 of operation. Drawing 10 is drawing showing the configuration setting table 57 which described two or more numbers of implementation which realize predetermined processings and those processings. The logical circuit data for performing predetermined processings 76 and 77 described by the configuration setting table 57 and the configuration setting table 57 and the I/O circuit data according to bit width of face are memorized by the storage means 4.

[0062] Drawing 11 is the mimetic diagram showing the relation of the logical circuit data for performing predetermined processings 76 and 77, and the I/O circuit data according to bit width of face. Since the number of implementation of the configuration setting table 57 shown in drawing 10 is 2, in drawing 11 , the logical circuits 21 and 24 for performing predetermined processing 76 are realized by the integrated circuits 11 and 14 which can be reconfigurated, and the logical circuits 25 and 28 for performing predetermined processing 77 are realized at the integrated circuits 15 and 18 which can be reconfigurated. Moreover, the I/O circuits 31, 35, 34, and 38 for 16-bit width of face (I/O circuit) are realized by the integrated circuits 11, 15, 14, and 18 which can be reconfigurated.
[0063] That is, when assigning the predetermined processing 76 to the integrated circuit 11 which can be reconfigurated and assigning the predetermined processing 77 to the integrated circuit 15 which can be reconfigurated, the instruction control means 2 compounds the logical circuit 21 for performing predetermined processing 76, and the I/O circuit 31 for 16 bit width of face, writes in the integrated circuit 11 which can be reconfigurated, compounds the logical circuit 25 for performing predetermined processing 77, and the I/O circuit 35 for 16 bit width of face, and writes in to the integrated circuit 15 which can be reconfigurated.
[0064] When similarly assigning the predetermined processing 76 to the integrated circuit 14 which can be reconfigurated and assigning the predetermined processing 77 to the integrated circuit 18 which can be reconfigurated, the instruction control means 2 compounds a logical circuit 24 and the I/O circuit 34 for 16-bit width of face, is written in the integrated circuit 14 which can be reconfigurated, compounds a logical circuit 28 and the I/O circuit 38 for 16-bit width of face, and writes them in the integrated circuit 18 which can be reconfigurated.
[0065] While exchanging the data of 16-bit width of face twice among the integrated circuits 11 and 15 which can be reconfigurated since the signal line of 32-bit width of face is needed for exchange of the data of the predetermined processings 76 and 77 as shown in the configuration setting table 57 of drawing 10 , the data of 16-bit width of face are exchanged twice among the integrated circuits 14 and 18 which can be reconfigurated. In this case, the logical circuits 21 and 24 corresponding to the predetermined processing 76 exchange data for the logical circuits 25 and 28 corresponding to the predetermined processing 77 through the I/O circuits 31 and 35 for 16-bit width of face, and the I/O circuits 34 and 38 for 16-bit width of face, respectively.
[0066] Since the logical circuits 21 and 24 corresponding to the processing 76 predetermined to the above-mentioned case are common logical circuits and are logical circuits where the logical circuits 25 and 28 corresponding to the predetermined processing 77 are also common, By dividing and writing logical circuits 21, 25, 24, and 28 and the I/O circuits 31, 35, 34, and 38 for 16-bit width of face in the integrated circuits 11, 15, 14, and 18 which can be reconfigurated It is not necessary to create logical circuits 21 and 24 separately and to also create logical circuits 25 and 28 separately.
[0067] Drawing 12 is another mimetic diagram showing the relation of the logical circuit data for performing predetermined processings 76 and 77, and the I/O circuit data according to bit width of face. In drawing 12 , the logical circuits 22 and 23 corresponding to the predetermined processing 76 are realized by the integrated circuits 12 and 13 which can be reconfigurated, and the logical circuits 26 and 27 for performing predetermined processing 77 are realized at the integrated circuits 16 and 17 which can be reconfigurated. Moreover, the I/O circuits 32, 36, 33, and 37 for 8-bit width of face (I/O circuit) are realized by the integrated circuits 12, 16, 13, and 17 which can be reconfigurated.
[0068] Since the signal line of 32-bit width of face is needed for exchange of the data of the predetermined processings 76 and 77, the data of 8-bit width of face are exchanged by a unit of 4 times, respectively between the integrated circuits 12 and 16 which can be reconfigurated, and the integrated circuits 13 and 17 which can be reconfigurated. In this case, the logical circuits 22 and 23 for performing predetermined processing 76 exchange data for the logical circuits 26 and 27 for performing predetermined processing 77 through the I/O circuits 32, 36, 33, and 37 for 8-bit width of face, respectively.
[0069] Since the logical circuits 22 and 23 for performing predetermined processing 76 in the above-mentioned case are common logical circuits and are logical circuits where the logical circuits 26 and 27

for performing predetermined processing 77 are also common, By dividing and writing logical circuits 22, 26, 23, and 27 and the I/O circuits 32, 36, 33, and 37 for 8-bit width of face in the integrated circuits 12, 16, 13, and 17 which can be reconfigurated It is not necessary to create logical circuits 22 and 23 separately and to also create logical circuits 26 and 27 separately.

[0070] Moreover, when exchanging data by the predetermined processings 76 and 77, since the 16-bit width-of-face signal line can exchange many data at a time rather than a 8-bit width-of-face signal line, it is advantageous. The circuitry management tool 3 may assign circuitry data to the more advantageous integrated circuits 11-18 which can be reconfigurated based on the information on the bit width of face of such a signal line. In the above-mentioned example, the direction assigned, for example as shown in drawing 11 rather than drawing 12 can accelerate predetermined processing. Thus, predetermined processing is accelerable by assigning predetermined processing to the larger thing of the data-exchange capacity between [which can be reconfigurated] integrated circuits 11-18.

[0071] As mentioned above, according to the gestalt 5 of this operation, the effectiveness that it is not necessary to create a common logical circuit separately is acquired by dividing and writing a logical circuit and an I/O circuit in the integrated circuits 11-18 which can be reconfigurated.

[0072] Moreover, according to the gestalt 5 of this operation, when the circuitry management tool 3 assigns circuitry data to the large integrated circuits 11-18 of bit width of face which can be reconfigurated based on the information on the bit width of face of the signal line of the integrated circuits 11-18 which can be reconfigurated, the effectiveness that predetermined processing is accelerable is acquired.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the configuration of the parallel computer by the gestalt 1 of implementation of this invention which can be reconfigurated.
[Drawing 2] It is drawing showing the configuration setting table which described the number of implementation of the reconstruction integrated circuit which performs predetermined processing by the gestalt 1 of implementation of this invention, and its processing.
[Drawing 3] It is drawing showing the configuration setting table which described the number of implementation of the reconstruction integrated circuit which performs predetermined processing by the gestalt 2 of implementation of this invention, and its processing.
[Drawing 4] It is drawing showing the configuration setting table which described the number of implementation of the reconstruction integrated circuit which performs predetermined processing by the gestalt 2 of implementation of this invention, and its processing.
[Drawing 5] It is drawing showing the configuration setting table which described the number of implementation of the reconstruction integrated circuit which performs predetermined processing by the gestalt 2 of implementation of this invention, and its processing.
[Drawing 6] It is drawing showing the configuration of the parallel computer by the gestalt 3 of implementation of this invention which can be reconfigurated.
[Drawing 7] It is drawing showing the configuration setting table which described the number of implementation of the reconstruction integrated circuit which performs predetermined processing by the gestalt 3 of implementation of this invention, and its processing.
[Drawing 8] It is drawing showing the configuration of the parallel computer by the gestalt 4 of implementation of this invention which can be reconfigurated.
[Drawing 9] It is drawing showing the configuration setting table which described the number of implementation of the reconstruction integrated circuit which performs predetermined processing by the gestalt 4 of implementation of this invention, and its processing.
[Drawing 10] It is drawing showing the configuration setting table which described the number of implementation of the reconstruction integrated circuit which performs predetermined processing by the gestalt 5 of implementation of this invention, and its processing.
[Drawing 11] It is the mimetic diagram showing the relation between the logical circuit data based on the gestalt 5 of implementation of this invention, and the I/O circuit data according to bit width of face.
[Drawing 12] It is the mimetic diagram showing the relation between the logical circuit data based on the gestalt 5 of implementation of this invention, and the I/O circuit data according to bit width of face.
[Drawing 13] It is drawing showing the configuration of the conventional parallel computer which can be reconfigurated.
[Description of Notations]
1 The parallel computer which can be reconfigurated, 2 An instruction control means, 3 A circuitry management tool, 4 storage means, 11-18 The integrated circuit which can be reconfigurated, 51-57 A configuration setting table, 21-28 A logical circuit, 31, 34, 35, 38 The I/O circuit for 16-bit width of face

(I/O circuit), 32, 33, 36, 37 I/O circuit for 8-bit width of face (I/O circuit).

[Translation done.]

* NOTICES *

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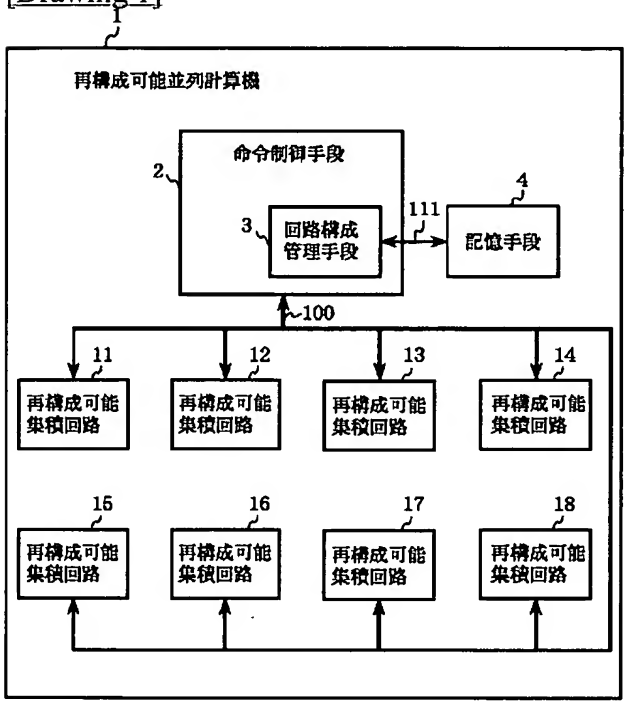
DRAWINGS

[Drawing 1]



[Drawing 2]

構成設定テーブル51

処理	実現数
処理61	5
処理62	2

[Drawing 3]

構成設定テーブル52
実行開始時間=0

処理	実現数
処理63	3
処理64	2

[Drawing 4]

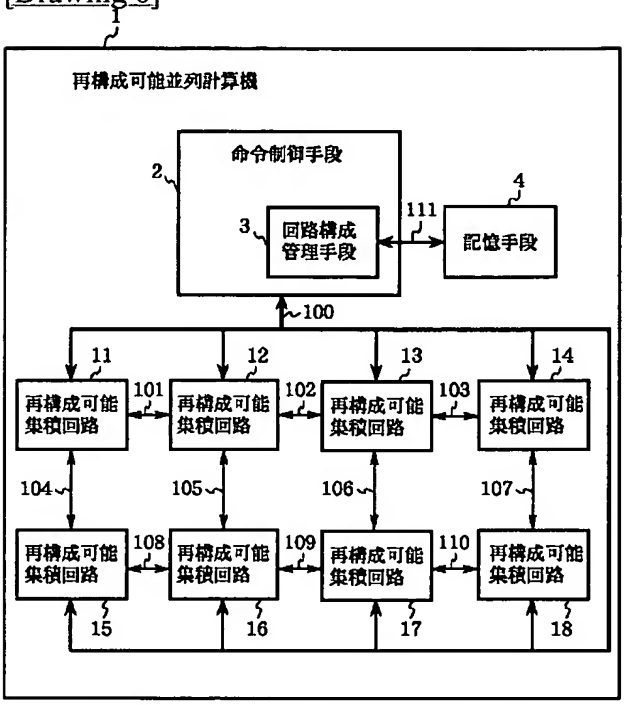
構成設定テーブル53
実行開始時間＝100

処理	実現数
処理65	3

[Drawing 5]
構成設定テーブル54
実行開始時間＝1

処理	実現数
処理66	5

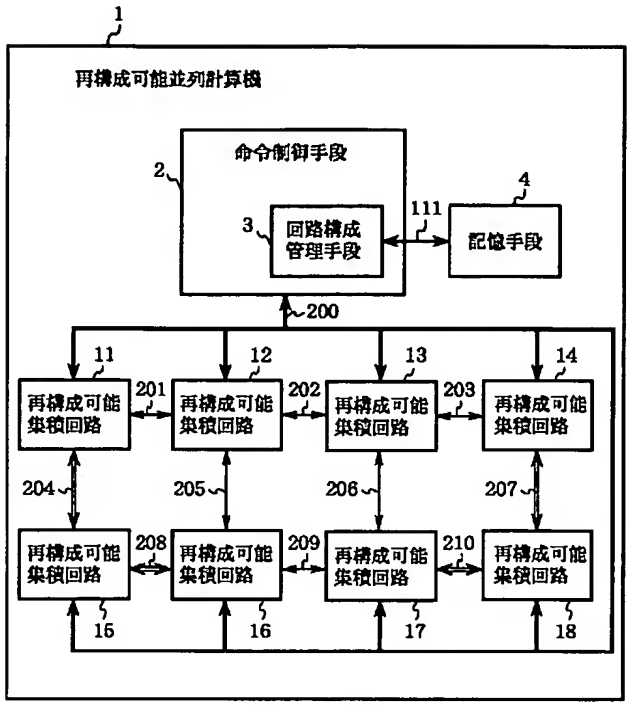
[Drawing 6]



[Drawing 7]
構成設定テーブル55

処理	実現数
データ入力 ↓ 処理67 ↙ ↘ 処理68 処理69 ↘ ↙ 処理70 ↓ データ出力	1
処理71	3

[Drawing 8]



[Drawing 9]

構成設定テーブル56

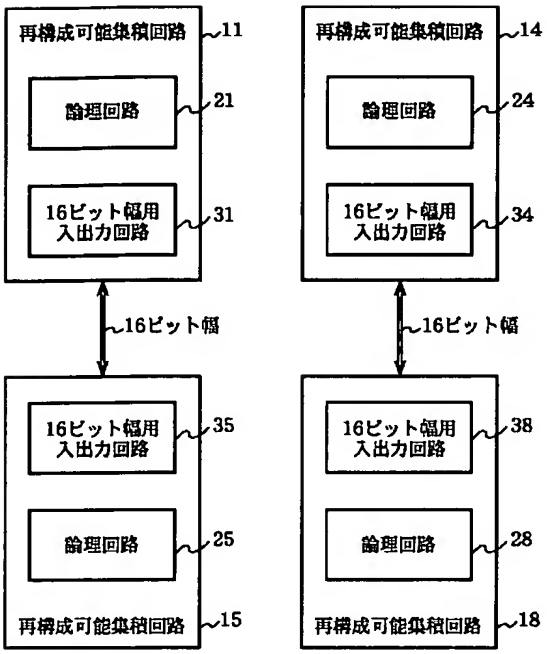
処理	実現数
データ入力 ↓ 処理72 ↓(16) 処理73 ↓(16) 処理74 ↓(8) 処理75 ↓ データ出力	2

[Drawing 10]

構成設定テーブル57

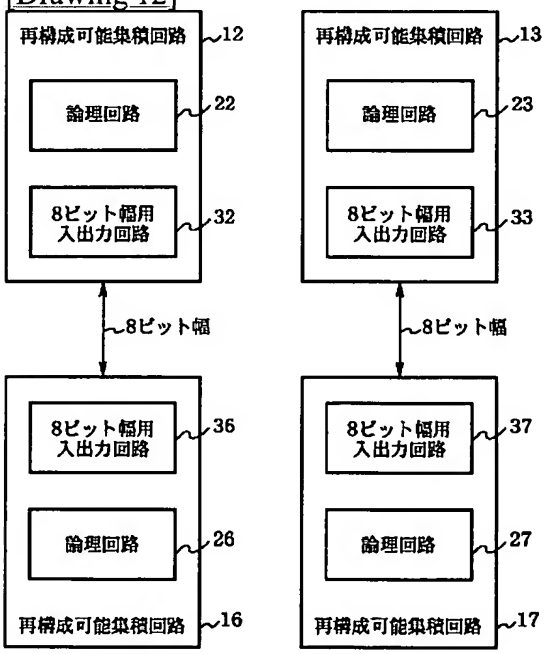
処理	実現数
データ入出力 ↓ ↑ 処理76 ↓ ↑(32) 処理77	2

[Drawing 11]



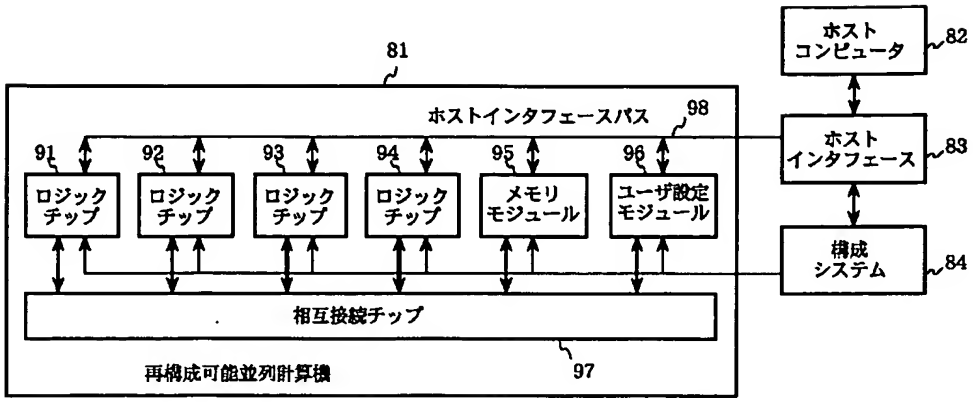
31,34,35,38 : 16ビット幅用入出力回路（入出力回路）

[Drawing 12]



32,33,36,37 : 8ビット幅用入出力回路（入出力回路）

[Drawing 13]



[Translation done.]